BTD25350x

Dual-Channel Isolated Gate Driver

1.Features

- Isolation voltage up to 5000Vrms
- Peak output current up to 10A
- Propagation delay 40ns
- Maximum switching frequency 1MHz
- Primary-side supply 3~5V
- Secondary-side supply up to 33V
- Primary-side and secondary-side power supply undervoltage lockout (UVLO)
- Compatible with 3.3V, 5V input
- Feature Options:
  Miller Clamp Options (BTD25350MM)
  Split Outputs (BTD25350MS)
  UVLO referenced to secondary side GNDx (BTD25350ME)
- SOW-18 with 8.5mm creepage
- Operating Temperature -40~125°C

2.Applications

- Motor drives
- EV chargers
- Telecommunication power supplies
- EV power supplies
- UPS
- String solar inverters

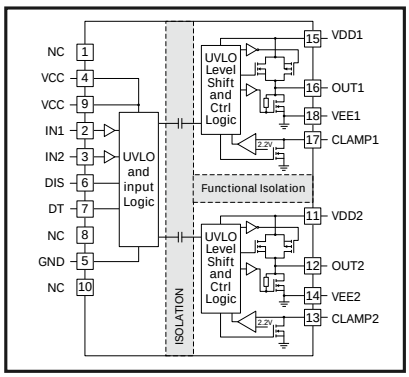
3.Description

BTD25350x is a family of dual-channel, isolated gate driver with peak output current up to 10A, available in SOW-18 (wide-body) package and supports isolation voltages up to 5000Vrms. They can be used to drive IGBTs and Si/SiC MOSFETs. BTD25350x family offers 3 Feature Options:
BTD25350MM provides Miller clamp function to prevent false turn-on caused by Miller current.
BTD25350MS provides a split output with rise and fall time individually configurable.
BTD25350ME provides UVLO in positive power supply of secondary-side to ensure that power devices get sufficient gate turn-on voltage.

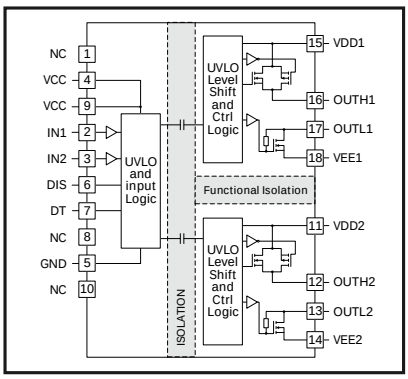
RoHS
COMPLIANT

SOW-18

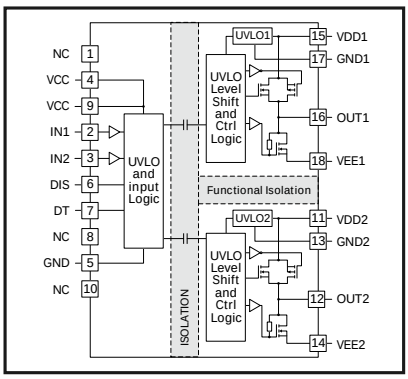
4.Functional Block Diagram



BTD25350MM



BTD25350MS



BTD25350ME

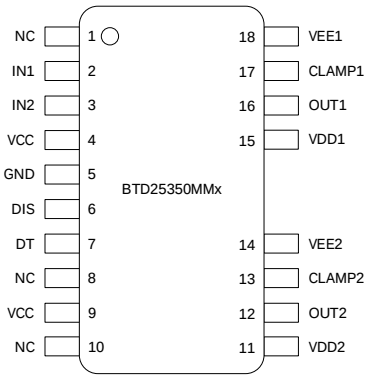
INDEX

5.Product Information

Part No.	Pin Configuration	Isolation Voltage	UVLO Threshold	Operating Temperature	Package	Package Material	Quantity	Marking
BTD25350MMBWR	dead time configuration and disable function, Miller-clamp	5000Vrms	8V	-40~125°C	SOW-18	Tape & Reel	1500pcs /Reel	BTD25350MMB
BTD25350MMCWR			11V					BTD25350MMC
BTD25350MSBWR	dead time configuration and disable function, split output		8V					BTD25350MSB
BTD25350MSCWR			11V					BTD25350MSC
BTD25350MEBWR	dead time configuration and disable function, UVLO with reference to GNDx		8V					BTD25350MEB
BTD25350MECWR			11V					BTD25350MEC

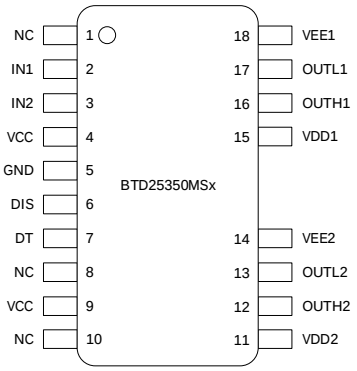
6.Pin Configuration and Functions

6.1 BTD25350MMx

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	NC	-	No internal connection	
2	IN1	I	Signal input channel 1	
3	IN2	I	Signal input channel 2	
4	VCC	P	Primary-side supply voltage	
5	GND	G	Primary side ground	
6	DIS	I	Disables both driver outputs if asserted high, enables if set low or left open	
7	DT	I	Programmable dead time function	
8	NC	-	No internal connection	
9	VCC	P	Primary-side supply voltage	
10	NC	-	No internal connection	
11	VDD2	P	Channel 2 positive output supply rail	
12	OUT2	O	Channel 2 gate-drive output	
13	CLAMP2	I	Channel 2 Miller-clamp input	
14	VEE2	P	Channel 2 negative output supply rail	
15	VDD1	P	Channel 1 positive output supply rail	
16	OUT1	O	Channel 1 gate-drive output	
17	CLAMP1	I	Channel 1 Miller-clamp input	
18	VEE1	P	Channel 1 negative output supply rail	

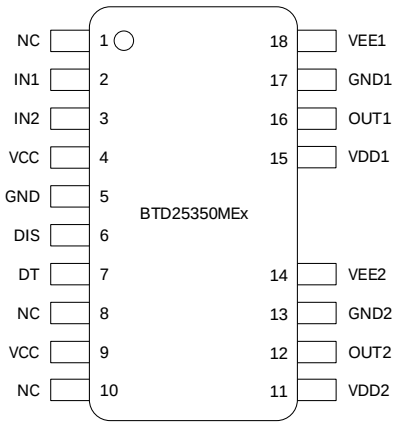
(1) P=Power, G=Ground, I=Input, O=Output

6.2 BTD25350MSx

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	NC	-	No internal connection	
2	IN1	I	Signal input channel 1	
3	IN2	I	Signal input channel 2	
4	VCC	P	Primary-side supply voltage	
5	GND	G	Primary-side ground reference	
6	DIS	I	Disables both driver outputs if asserted high, enables if set low or left open	
7	DT	I	Programmable dead time function	
8	NC	-	No internal connection	
9	VCC	P	Primary-side supply voltage	
10	NC	-	No internal connection	
11	VDD2	P	Channel 2 positive output supply rail	
12	OUTH2	O	Channel 2 gate-drive pullup output	
13	OUTL2	O	Channel 2 gate-drive pulldown output	
14	VEE2	P	Channel 2 negative output supply rail	
15	VDD1	P	Channel 1 positive output supply rail	
16	OUTH1	O	Channel 1 gate-drive pullup output	
17	OUTL1	O	Channel 1 gate-drive pulldown output	
18	VEE1	P	Channel 1 negative output supply rail	

(1) P=Power, G=Ground, I=Input, O=Output

6.2 BTD25350MEx

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	NC	-	No internal connection	
2	IN1	I	Signal input channel 1	
3	IN2	I	Signal input channel 2	
4	VCC	P	Primary-side supply voltage	
5	GND	G	Primary-side ground reference	
6	DIS	I	Disables both driver outputs if asserted high, enables if set low or left open	
7	DT	I	Programmable dead time function	
8	NC	-	No internal connection	
9	VCC	P	Primary-side supply voltage	
10	NC	-	No internal connection	
11	VDD2	P	Channel 2 positive output supply rail	
12	OUT2	O	Channel 2 gate-drive output	
13	GND2	G	Channel 2 gate-drive common	
14	VEE2	P	Channel 2 negative output supply rail	
15	VDD1	P	Channel 1 positive output supply rail	
16	OUT1	O	Channel 1 gate-drive output	
17	GND1	G	Channel 1 gate-drive common	
18	VEE1	P	Channel 1 negative output supply rail	

(1) P=Power, G=Ground, I=Input, O=Output

7. Specification Parameters

7.1 Absolute Limits

SYMBOL	PARAMETER	MIN	MAX	UNIT
VCC	Input bias pin supply voltage (pin 3/pin 8)	GND-0.3	6.5	V
VDDx	Driver bias supply (to VEEx)	0	35	
VEEx	Bipolar supply voltage for E version	-17.5	0.3	
V_{OUTx}	Output signal voltage	VEEx-0.3	VDDx+0.3	
V_{IN}	Input signal voltage (INx, DT, DIS to GND)	GND-0.3	VCC+0.3	
-	Channel to channel voltage	-	1850	
T_J	Junction Temperature	-40	150	°C
T_S	Storage Temperature	-65	150	
T_L	Soldering Temperature (10s)	-	300	
$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±3000		V
	Charge-device model (CDM), per ANSI/ESDA/JEDEC JS-002	±1500		
-	Input signal voltage(IN1,IN2 Transient for 50ns)	-5	VCC+0.3	
Note: The above are stress levels only.Devices are not recommended to operate under these or any other conditions beyond these values.Prolonged operation under the absolute maximum rating may affect the reliability of the device, and in severe cases it may cause permanent damage to the devices.				

7.2 Thermal Information

SYMBOL	DESCRIPTION	SOW-18	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.14	°C /W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.61	
$R_{\theta JB}$	Junction-to-board thermal resistance	37.53	
ψ_{JT}	Junction-to-top characterization parameter	4.88	
ψ_{JB}	Junction-to-board characterization parameter	9.59	

7.3 Power Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	SOW-18	UNIT
P_D	Power dissipation by BTD25350x	VCC=5V, VDD1/2=12V, IN1/2=3.3V, 3MHz, 50% duty cycle square wave, 1nF load	2.03	W
P_{D1}	Power dissipation by each driver side of BTD25350x		0.99	
P_{D2}			0.99	
P_{DI}	Power dissipation by transmitter side of BTD25350x		0.05	

7.4 Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC}	Input supply voltage (VCC-GND)		3	5	V
V_{DDx}	Total supply voltage output side (VDDx-VEEx)	BTD25350xBx	9.5	33	
		BTD25350xCx	13.2	33	
V_{EEx}	Bipolar supply voltage for E version (VEEx–GNDx)		-16	0	
T_A	Ambient temperature		-40	125	°C

7.5 Safety-Limiting Values

SYMBOL	PARAMETER	TEST CONDITIONS		SIDE	MIN	MAX	UNIT
I_S	Safety output supply current	T_A=25°C , T_J= 150°C	VDD1/2=12V	CHANNEL1, CHANNEL2	-	87.5	mA
			VDD1/2=25V	CHANNEL1, CHANNEL2	-	42	
P_S	Safety supply power	VDD1/2=25V, T_A=25°C , T_J=150°C		INPUT	-	50	mW
				CHANNEL1	-	1050	
				CHANNEL2	-	1050	
				TOTAL	-	2150	
T_S	Safety temperature (1)				-	150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

7.6 Electrical Characteristics

T_A=-40~125°C , V_{CC}=3.3 or 5V, V_{DDx}=15V, C_L=100pF.
Output pin: current towards outside of the chip is positive direction; Input pin: current towards inside of the chip is positive direction.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Currents						
I_{VCCQ}	Primary side input supply quiescent current	V_{DDx}=15V, V_{IN1}=V_{IN2}=0V	-	1.5	2	mA
$I_{VCCQ-ST}$	Primary side input supply current	V_{IN1}=V_{IN2}=5V, f=500kHz, C_L=100pF, D=50%	-	2	-	
Primary Side Undervoltage Lockout						
V_{ON_VCC}	Positive-going UVLO threshold voltage	-	-	2.6	-	V
V_{OFF_VCC}	Negative-going UVLO threshold voltage	-	-	2.5	-	
$V_{UV\_HYS\_VCC}$	Threshold hysteresis	-	-	0.1	-	
Secondary Side Undervoltage Lockout						
V_{ON_VDDx}	Rising threshold	BTD25350xxC	-	12	13	V
V_{OFF_VDDx}	Falling threshold		10.3	11	-	
V_{UV_HYSx}	Threshold hysteresis		-	1	-	
V_{ON_VDDx}	Rising threshold	BTD25350xxB	-	8.7	9.4	
V_{OFF_VDDx}	Falling threshold		7.3	8	-	
V_{UV_HYSx}	Threshold hysteresis		-	0.7	-	
Input Characteristics						
V_{IH}	Input logic 1 (INx, DIS)	V_{CC}=5V	-	2.4	-	V
V_{IL}	Input logic 0 (INx, DIS)	V_{CC}=5V	-	1.4	-	
V_{I_HYS}	Input hysteresis voltage	-	-	1	-	
I_{IH}	High-level input leakage at IN+	INx=3.3V	-	15	-	µA
		INx=5V	-	25	-	
I_{IL}	Low-level input leakage at IN-	INx=GND	-	-	5	
Output Characteristics						
I_{OH}	Peak output source current	-	-	10	-	A
I_{OL}	Peak output sink current	-	-	10	-	
V_{OH}	Output voltage at high state (OUTx, OUTHx)	I_{OUT}=20mA	-	VDDx-0.06	-	V
V_{OL}	Output voltage at low state (OUTx, OUTLx)	I_{OUT}=-20mA	VEEx+0.005	VEEx+0.007	-	
Miller Clamp BTD25350MMxx						
V_{CLAMP}	Low-level clamp voltage	I_{CLAMP}=-20mA	-	7	10	mV
I_{CLAMP}	Low-level clamp current	V_{CLAMP}=VEEx+15V	-	10	-	A
V_{CLAMP_TH}	Clamping threshold voltage	-	-	2.2	-	V

(Continued)

Short-Circuit Clamping							
$V_{CLP-OUT}$	Clamping voltage (VOUTx-VDDx or VOUTHx-VDDx)		INx=HIGH, t_{CLAMP}=10μs, I_{OUTHx} or I_{OUTx}=-500mA	-	1	1.3	V
	Clamping voltage (VEEx-VOUTx or VEEx-VOUTLx or VEEx-CLAMPx)		INx=LOW, t_{CLAMP}=10μs, I_{CLAMPx} or I_{OUTLx}=500mA	-	1.5	-	
			INx=LOW， I_{CLAMPx} or I_{OUTLx}=20mA	-	0.9	1	
Active Pull-Down Function							
V_{OUTSD}	Active pulldown voltage on OUTLx, CLAMPx, OUTx		I_{OUT}=-1A (sinking into OUTx, OUTLx or CLAMPx pin), VDDx=left open	-	2.3	-	V
Switching Parameters							
t_{PLH}	Turn-on delay (INx to OUTx)		C_L=100pF	-	40	-	ns
t_{PHL}	Turn-off delay (INx to OUTx)		C_L=100pF	-	45	-	
t_r	Output rise time		C_L=1nF	-	10	26	
t_f	Output fall time		C_L=1nF	-	10	26	
t_{PWD}	Pulse width distortion $\lvert t_{PHL}-t_{PLH}\rvert$		C_L=100pF	-	1	20	
t_{DM}	Propagation delays matching between VOUT1, VOUT2		f=100kHz, IN1=IN2	-	-	5	
DT	Dead time		DT pull up to VCC	Two output channels are completely independent			
			DT pin open (not recommended)	-	8	15	
			R_{DT}=20kΩ	-	200	-	
t_{sk}	Part-to-part skew		C_L=100pF	-	1	25	
$t_{UVLO1-rec}$	Undervoltage lockout recovery delay time	Input side	VCC	-	40	-	μs
$t_{UVLO2-rec}$		Output side	VDDx	-	50	-	
CMTI	Common-mode transient immunity		INx fixed to GND or VCC, V_{CM}=1500V	150	-	-	kV/μs

7.7 SAFETY PARAMETERS

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLR	External clearance	Shortest pin-to-pin distance through air	8.5	-	-	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	8.5	-	-	
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2×8.5 μm)	17	-	-	μm
CTI	Comparative tracking index	DIN EN 60112	600	-	-	V
-	Overvoltage category per IEC 60664-1	Voltage rating ⩽ 600Vrms	I-IV	-	-	-
		Voltage rating ⩽ 1000Vrms	I-III	-	-	
VDE 0884-11						
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	-	-	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB)	1500	-	-	Vrms
		DC voltage	2121	-	-	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST}=V_{IOTM}$, t=60s (qualification) $V_{TEST}=1.2\times V_{IOTM}$, t=1s （100% production）	7000	-	-	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	IEC 62368-1, 1.2/50μs waveform, $V_{TEST}=1.6\times V_{IOSM}=10000V_{PK}$ (qualification)	6250	-	-	
Q_{pd}	Apparent charge	Method a, After Input/Output safety test subgroup 2/3. $V_{INI}=V_{IOTM}$, t_{INI}=60s; $V_{pd(m)}=1.2\times V_{IORM}=2545V_{PK}$, tm=10s	-	-	5	pC
		Method a, After environmental tests subgroup 1. $V_{INI}=V_{IOTM}$, t_{INI}=60s; $V_{pd(m)}=1.6\times V_{IORM}=3394V_{PK}$, tm=10s	-	-	5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{INI}=1.2\times V_{IOTM}$, t_{INI}=1s; $V_{pd(m)}=1.875\times V_{IORM}=3977V_{PK}$, tm=1s	-	-	5	
C_{IO}	Barrier capacitance, input to output	$V_{IO}=0.4V_{peak}$, f=1MHz, sine wave	-	1.2	-	pF
R_{IO}	Isolation resistance, input to output	Test voltage of 500V, T_A=25°C	10^{12}	-	-	Ω
		Test voltage of 500V, 100°C⩽ T_A ⩽125°C	10^{11}	-	-	
		Test voltage of 500V, T_A=150°C	10^{9}	-	-	
	Pollution degree	-	-	2	-	-
	Climatic category	-	-	40/125/21	-	-
UL1577						
V_{ISO}	Withstand isolation voltage	$V_{TEST}=V_{ISO}$, t=60 sec(qualification); $V_{TEST}=1.2\times V_{ISO}$=6000Vrms, t=1 sec(100% production)	5000	-	-	Vrms

8.Parameter Testing

8.1 Propagation Delay

The method for measuring the rise time (t_r) and fall time (t_f) see Figure 1.

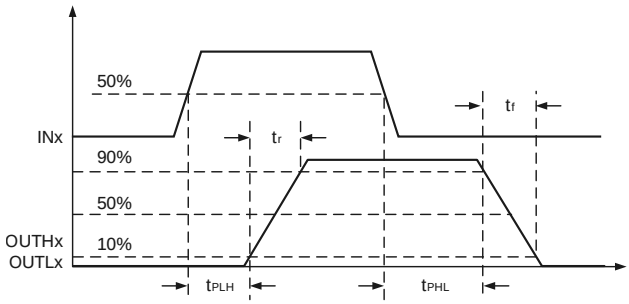


Figure 1. Input and Output Propagation Delay

8.2 CMTI

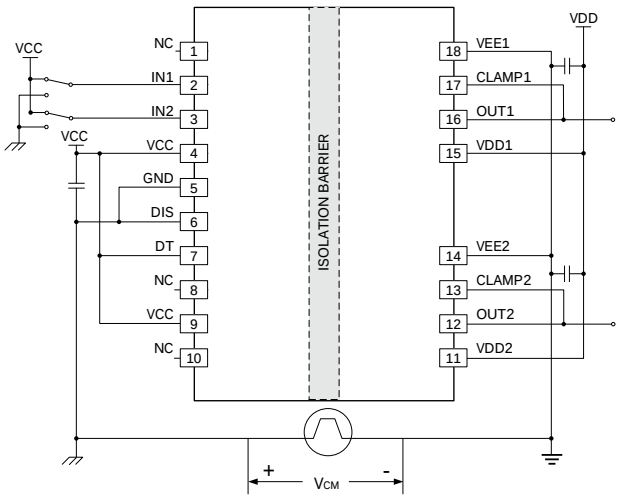


Figure 2. CMTI Test Circuit for BTD25350MMx

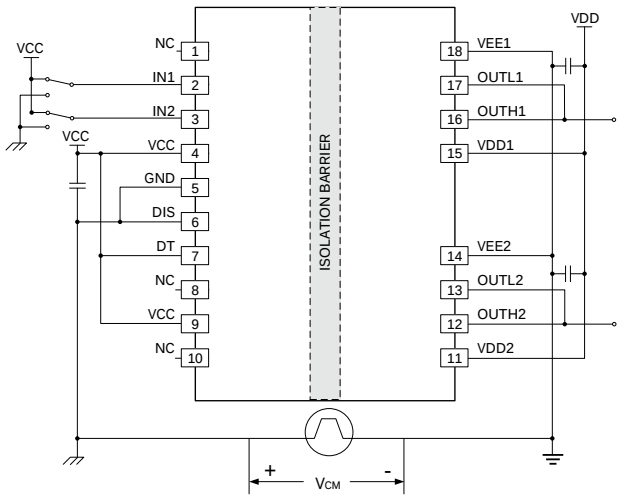


Figure 3. CMTI Test Circuit for BTD25350MSx

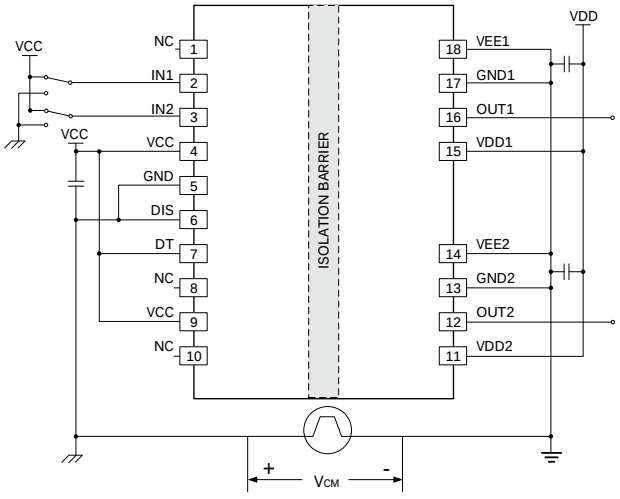


Figure 4. CMTI Test Circuit for BTD25350MEx

8.3 Typical Characteristics

T_A=-40~125℃ , V_{CC}=3.3V or 5V, V_{DDx}=15V, load capacitance C_L=100pF. unless otherwise indicated.

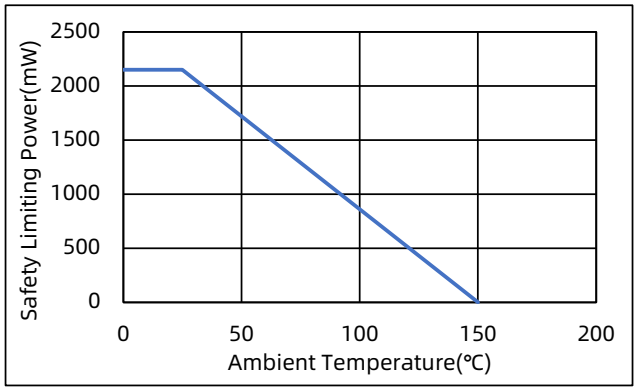


Figure 5. Temperature derating curve of safe power

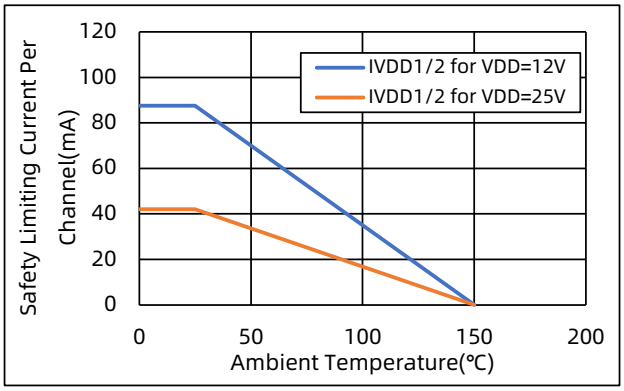


Figure 6. Temperature derating curve of safety current

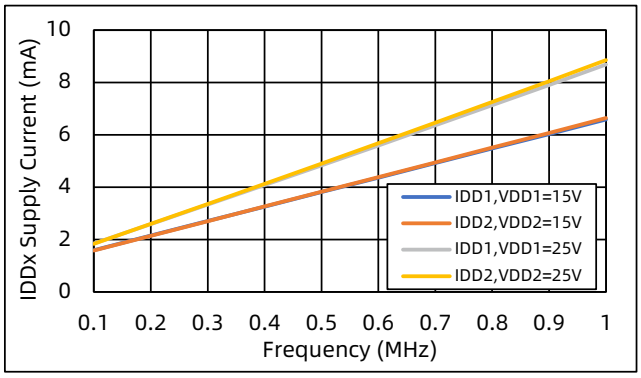


Figure 7. Single channel current consumption vs. Frequency (No load, VDD=12V or 25V)

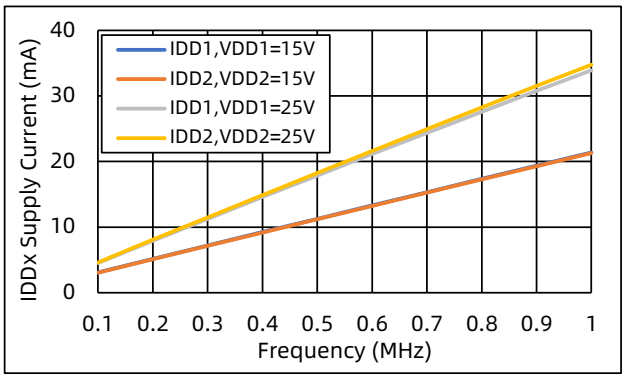


Figure 8. Single channel current consumption vs. Frequency (1nF load, VDD=12V or 25V)

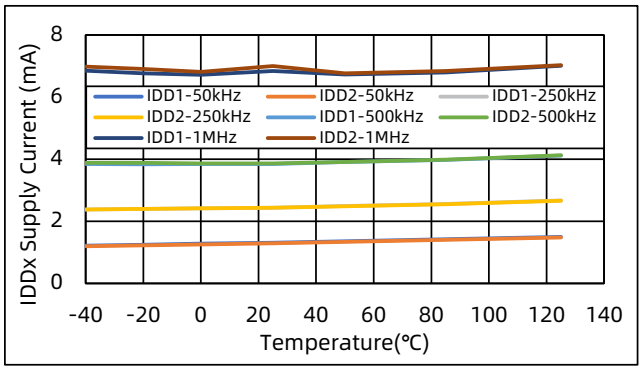


Figure 9. Single channel power supply current vs. temperature(No load, different switching frequency)

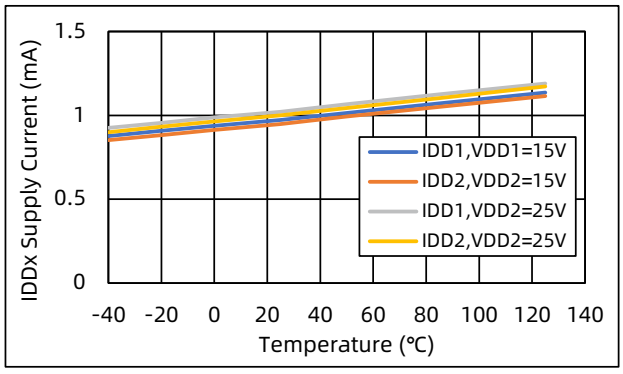


Figure 10. Secondary power supply per channel static current vs.temperature (No-load, input low level)

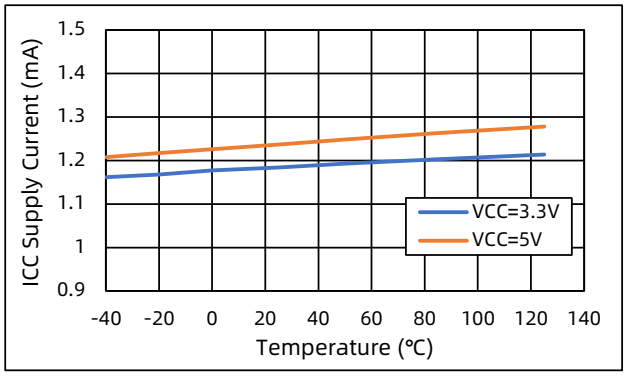


Figure 11. Ivcc static current vs. temperature (No-load, input low level)

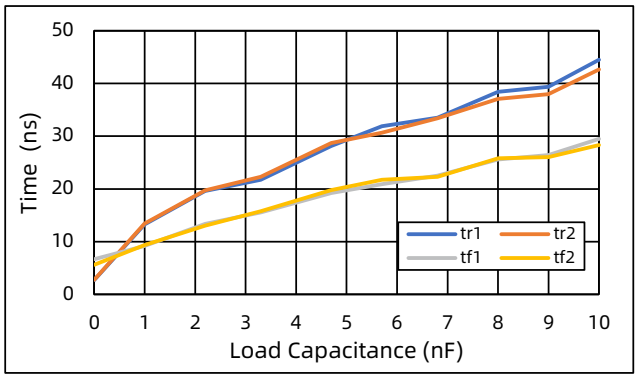


Figure 12. Rise and fall time vs. Load ($V_{VDD1/2}$=15V)

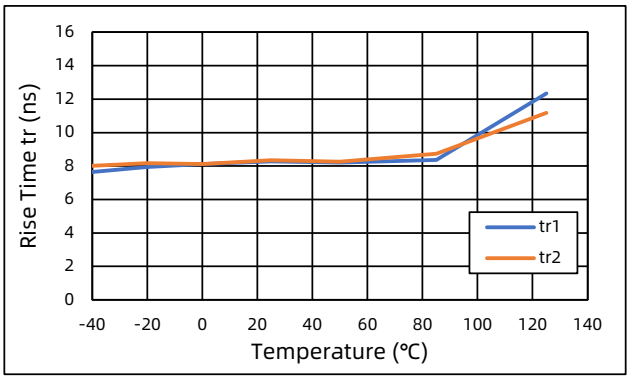


Figure 13. Rise time vs.temperature (1nF load)

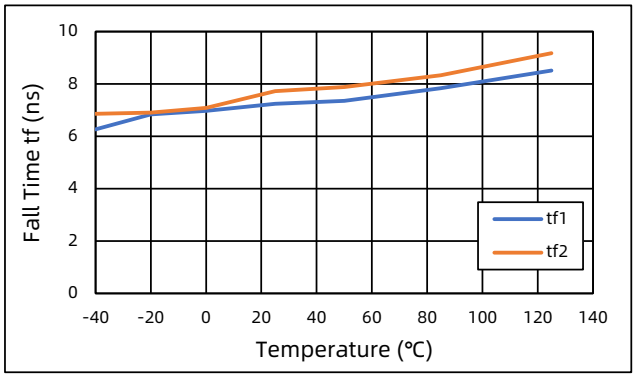


Figure 14. Fall time vs.temperature (1nF load)

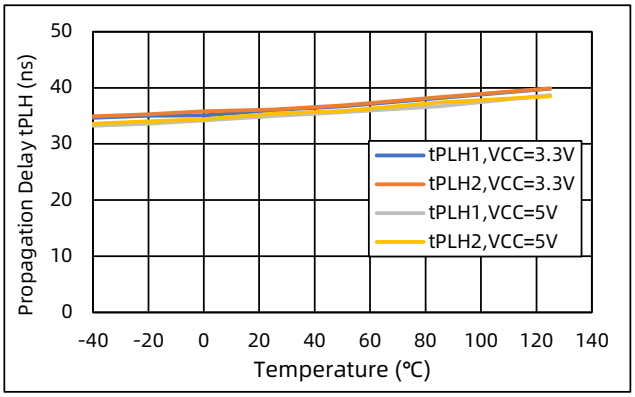


Figure 15. Transmission delay vs. temperature (1nF load)

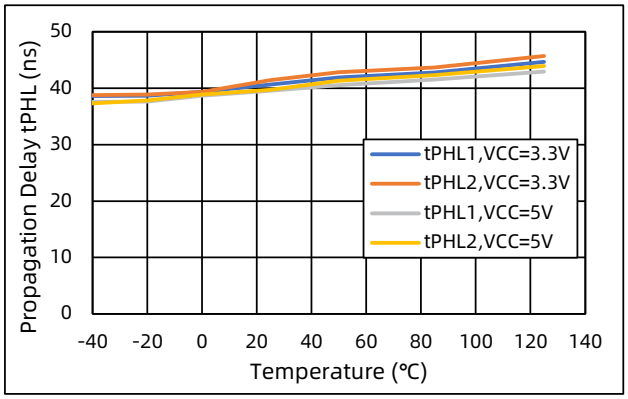


Figure 16 Transmission delay vs. temperature (1nF load)

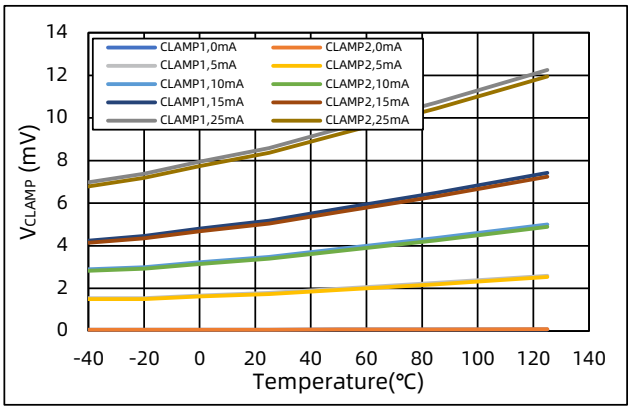


Figure 17. V_{CLAMP} vs. temperature (Input low level)

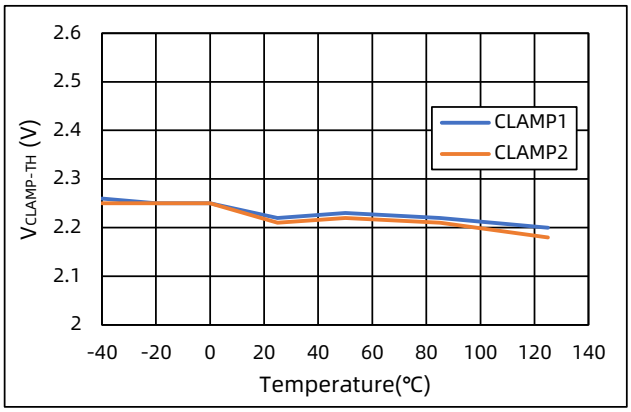


Figure 18. $V_{CLAMP-TH}$ vs. temperature

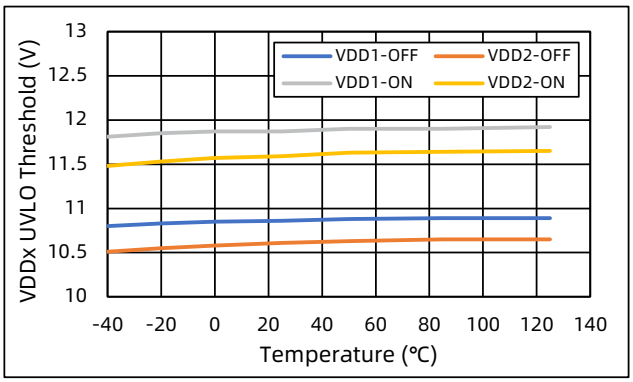


Figure 19. Secondary undervoltage threshold vs.temperature

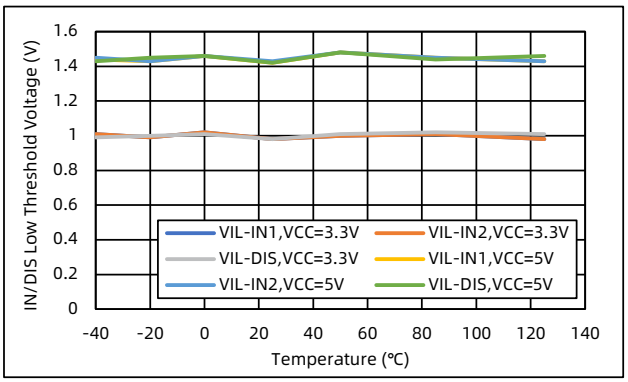


Figure 20. IN/DIS Low Level Threshold vs. Temperature

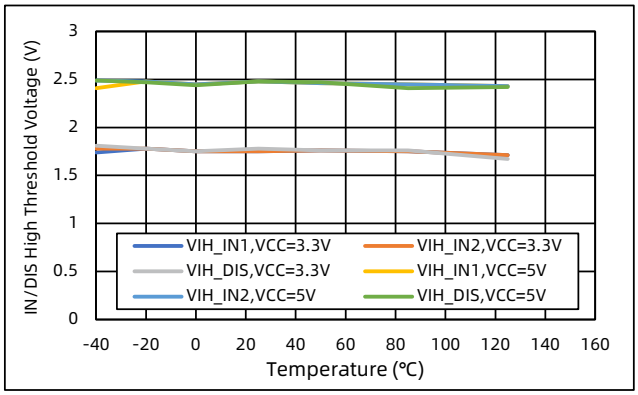


Figure 21. IN/DIS high level threshold vs.temperature

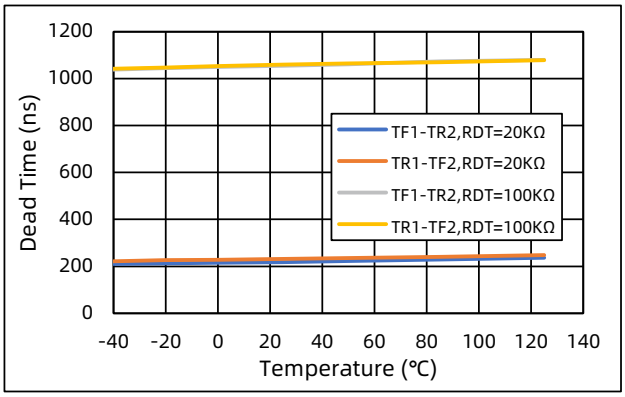


Figure 22. Dead time vs. Temperature (R_{DT}=20kΩ/100kΩ)

9.Function Description

9.1 Isolation Design Description

The isolation inside the BTD25350x series is implemented with high voltage SiO_2 based capacitors. There is a capacitor on each of the primary-side and secondary-side to enhance insulation. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data. The primary-side transmits a high-frequency carrier to represent one digital state, and sends no signal to represent the other digital state. On the secondary side, the receiver demodulates the signal and produces output for control. One can also add special anti-jamming circuit on the primary /secondary sides to enhance the CMTI performance and minimize the radiate emissions (see Figure 23, 24).

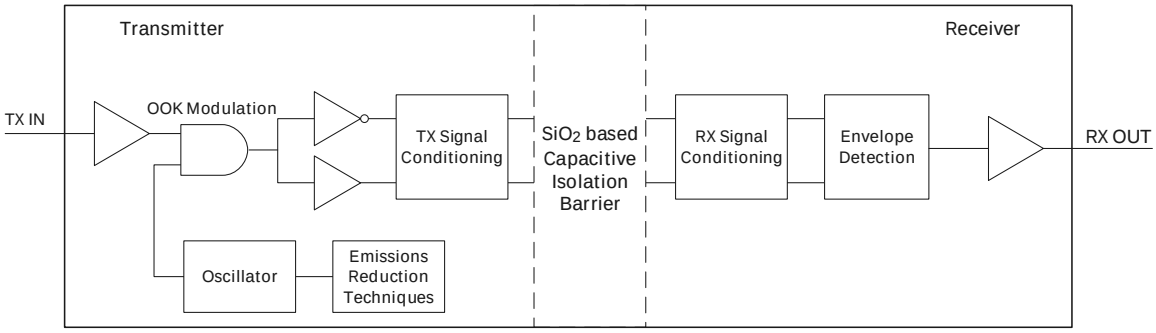


Figure 23. Conceptual Block Diagram of a Capacitive Data Channel

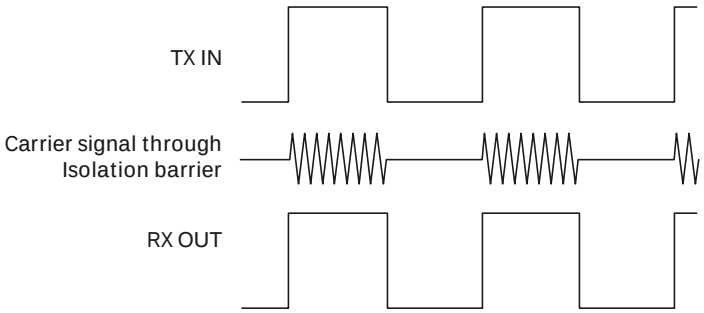


Figure 24. OOK Based Modulation Scheme

9.2 Input Stage Characteristics

With input pins and secondary side completely isolated, BTD25350x is designed to be CMOS-compatible. It supports 3.3V, 5V level input, making the chip easy to accept control of multiple logic levels. The input pin has Schmitt-trigger characteristic to enhance the immunity against disturbances. The INx and DIS input port has a 200kΩ pull-down resistor to force it grounding, which can ensure that the output ports are in OFF state when input ports are left open. However, in order to configure the initial power-on state of the driver IC, Recommends adding externally an appropriate pull-up or pull-down resistor to the input.

9.3 Primary Side Device Function

9.3.1 Disable

When the DIS pin is set to a high level, both outputs can be shut down at the same time. The device operates normally when the DIS pin is grounded or left open. The response time of the disable function is within 20ns. The disable function is activated or deactivated according to the setting only when the VCC is kept above the undervoltage turn-on threshold.

If the DIS pin is not used, it is recommended to connect it to the ground. If connecting DIS pin to a microcontroller with distance, it is recommended to bypass the DIS pin with a low ESR/ESL capacitor of approximately 1nF for better noise immunity.

9.3.2 Dead Time Setting

DT pin sets the dead time.It is used to set the dead time between channel 1 and channel 2 to prevent them from shoot-through. The steady-state voltage of DT pin is 0.8V, and the current value of the pin is measured for corresponding dead time. The dead time is calculated as $T_{DT}=10\times R_{DT}$. The unit of t_{DT} is ns and the unit of R_{DT} is kΩ. To ensure that the pin signal is not interfered, it is recommended to place a 2.2nF capacitor near the IC between DT pin and GND, and it is not recommended to left DT pin open.Pull DT up to VCC enables independent operation of two channels, no dead time is inserted, two outputs are allowed to be both high.

Figure 25. Dead Time Setting

9.4 Output Booster Characteristics

The BTD25350x has a rail-to-rail push stage output. The pull-up structure of the output stage consists of a P-channel MOSFET and an N-channel MOSFET connected in parallel. At turn-on, N-channel MOSFET provides high current driving capability. P-channel MOSFET provides a small steady-state conduction voltage drop during steady conduction. The pull-down structure is implemented using an N-channel MOSFET. A 1MΩ resistor is connected in parallel between the drain and gate of the MOSFET to effectively clamp the gate voltage of the power device in the event of a loss of power on the chip to prevent the occurrence of partial turn-on. However, in order to ensure reliable shutdown of the power device, BASiC recommends that appropriate pull-down resistor should be added to the gate.

It is recommended to connect Schottky clamping diode on the gate output for the positive supply VDDx and negative supply VEEx, in order to prevent gate transient over voltage.

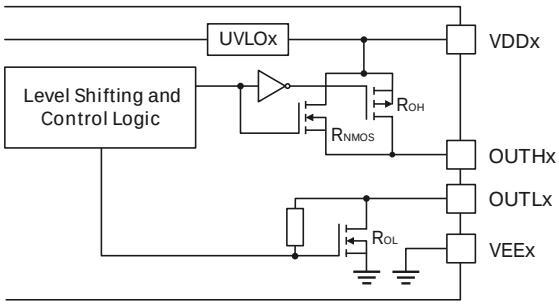


Figure 26. Output Stage

9.5 Protection Functions

9.5.1 Undervoltage Lockout

The BTD25350x has undervoltage lockout (UVLO) function on the primary-side power supply and the secondary-side total supply voltage to prevent the gate drive voltage from being insufficient. When the supply voltage drops below UVLO threshold, the IC turns off the output to protect the power devices. When the supply voltage reaches the positive-going negative-going threshold, the IC resumes the output. To prevent repeated action near the UVLO threshold, the IC is configured with hysteresis. In order to avoid the uncertainty of the output state after power-on, the IC first enters a UVLO state after power-on, keeps the output off until the supply voltage is established and then starts normal operation (see Figure 27).

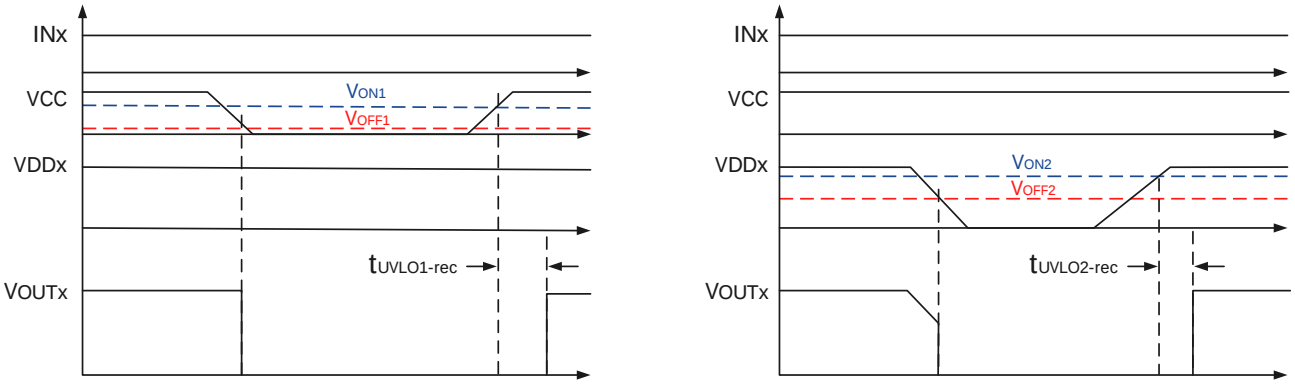


Figure 27. UVLO Functions

9.5.2 Miller Clamp

The active Miller clamp function is used to prevent the power devices from false turn-on of the power switched cause by the Miller current. A low impedance path is added between the gate terminal and ground (VEEx) to sink the Miller current. The Miller clamp function clamps the gate voltage of the power device to VEEx with the output is in the off state.

9.5.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the VDDx voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the VDDx pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10 μs and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

9.5.4 Active Pull-Down

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the VDDx. This feature prevents false IGBT and MOSFET turn-on on the OUTx, OUTLx and CLAMPx pins by clamping the output to approximately 2V.

9.6 ESD Structure

The figure below shows the ESD-protected diode configuration of the input and output pins.

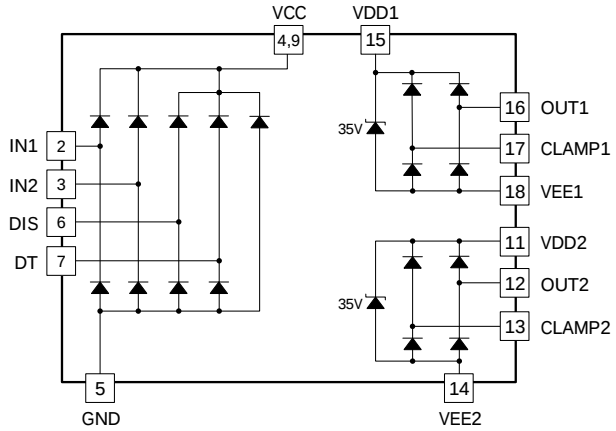


Figure 28. ESD Structure Diagram

9.7 Input and Output Logic Table

BTD25350MM 和 BTD25350ME

INPUT		DIS	OUTPUT		DESCRIPTION
IN1	IN2		OUT1	OUT2	
L	L	L or left open	L	L	If dead time function is used, output switching occurs after the dead time ended.See Programmable Dead Time (DT) pin
L	H	L or left open	L	H	
H	L	L or left open	H	L	
H	H	L or left open	L	L	Dead time stay open or programmed with R_{DT}
H	H	L or left open	H	H	Dead time pin pulled to VCC
Left open	Left open	L or left open	L	L	-
X	X	H	L	L	-

BTD25350MS

INPUT		DIS	OUTPUT				DESCRIPTION
IN1	IN2		OUTH1	OUTL1	OUTH2	OUTL2	
L	L	L or left open	Hi-Z	L	Hi-Z	L	If dead time function is used, output switching occurs after the dead time ended.See Programmable Dead Time (DT) pin
L	H	L or left open	Hi-Z	L	H	Hi-Z	
H	L	L or left open	H	Hi-Z	Hi-Z	L	
H	H	L or left open	Hi-Z	L	Hi-Z	L	Dead time stay open or programmed with R_{DT}
H	H	L or left open	H	Hi-Z	H	Hi-Z	Dead time pin pulled to VCC
Left open	Left open	L or left open	Hi-Z	L	Hi-Z	L	-
X	X	H	Hi-Z	L	Hi-Z	L	-

10.Applications

The following sections introduce the basic typical application of BASiC driver ICs, which is for reference only. In practical application, users need to verify and test its applicability according to their own design requirements to confirm the system functions.

10.1 Typical Applications

BASiC recommends that customers add a RC filter with a small time constant at the input port to filter out high-frequency interference without adding a large delay. It is recommended that the resistance value should be be-tween 0 and 100Ω and the capacitance should be less than 1000pF. When setting this parameter, the influence between high frequency interference and delay needs to be taken into account.

To ensure the supply stability, BASiC recommends to add appropriate blocking capacitor between the power supply and ground. It is recommended to parallel a 1μF+ 0.1μF capacitor between VCC-GND, and a 10μF+ 0.22μF capacitor between VDDx-VEEx (Figure 29,30,31).

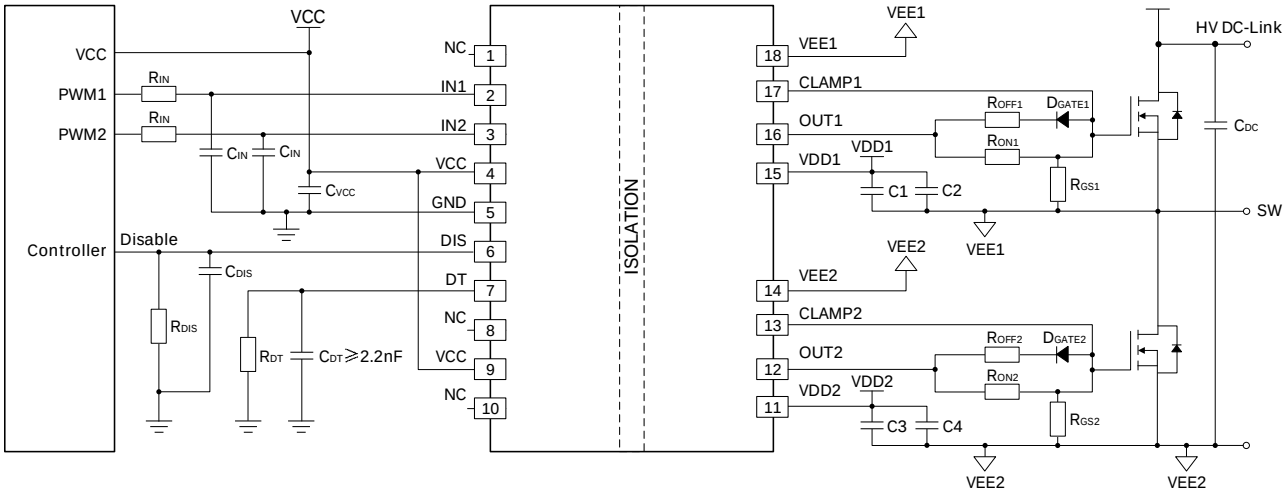


Figure 29. BTD25350MMx Application Diagram

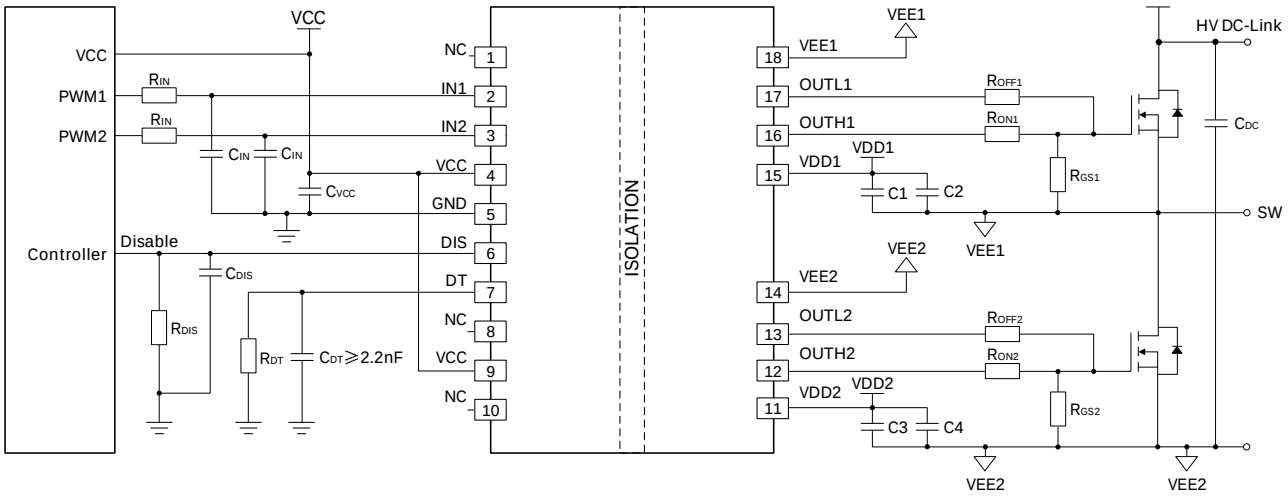


Figure 30. BTD25350MSx Application Diagram

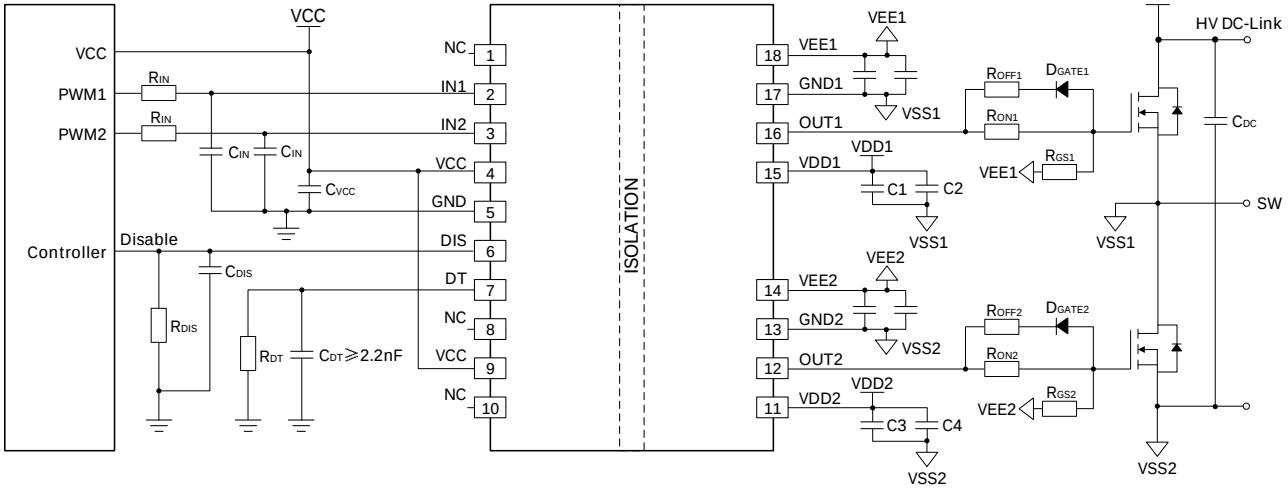


Figure 31. BTD25350MEx Application Diagram

10.2 Recommended Design of Secondary Side Supply

In order to avoid partial turn-on of the gate of the power device due to interference, it is recommended that customers add a negative supply when designing the driving output.It is recommended to use the following two methods to generate the negative supply: use a regulator to generate stable negative voltage, or use both positive and negative supplies.

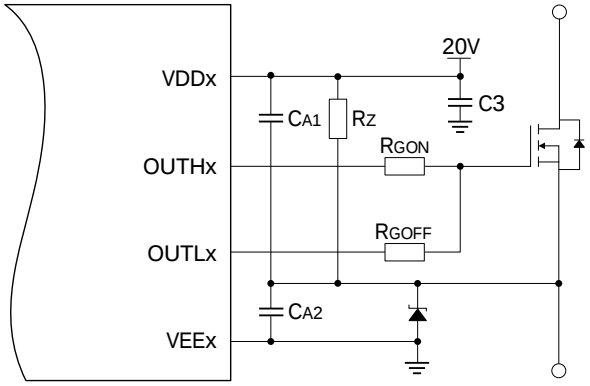


Figure 32. Voltage Regulator Design

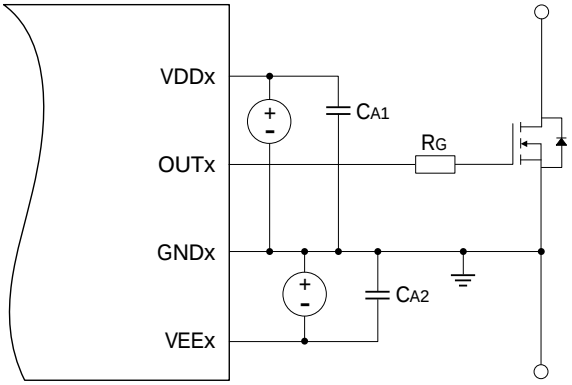
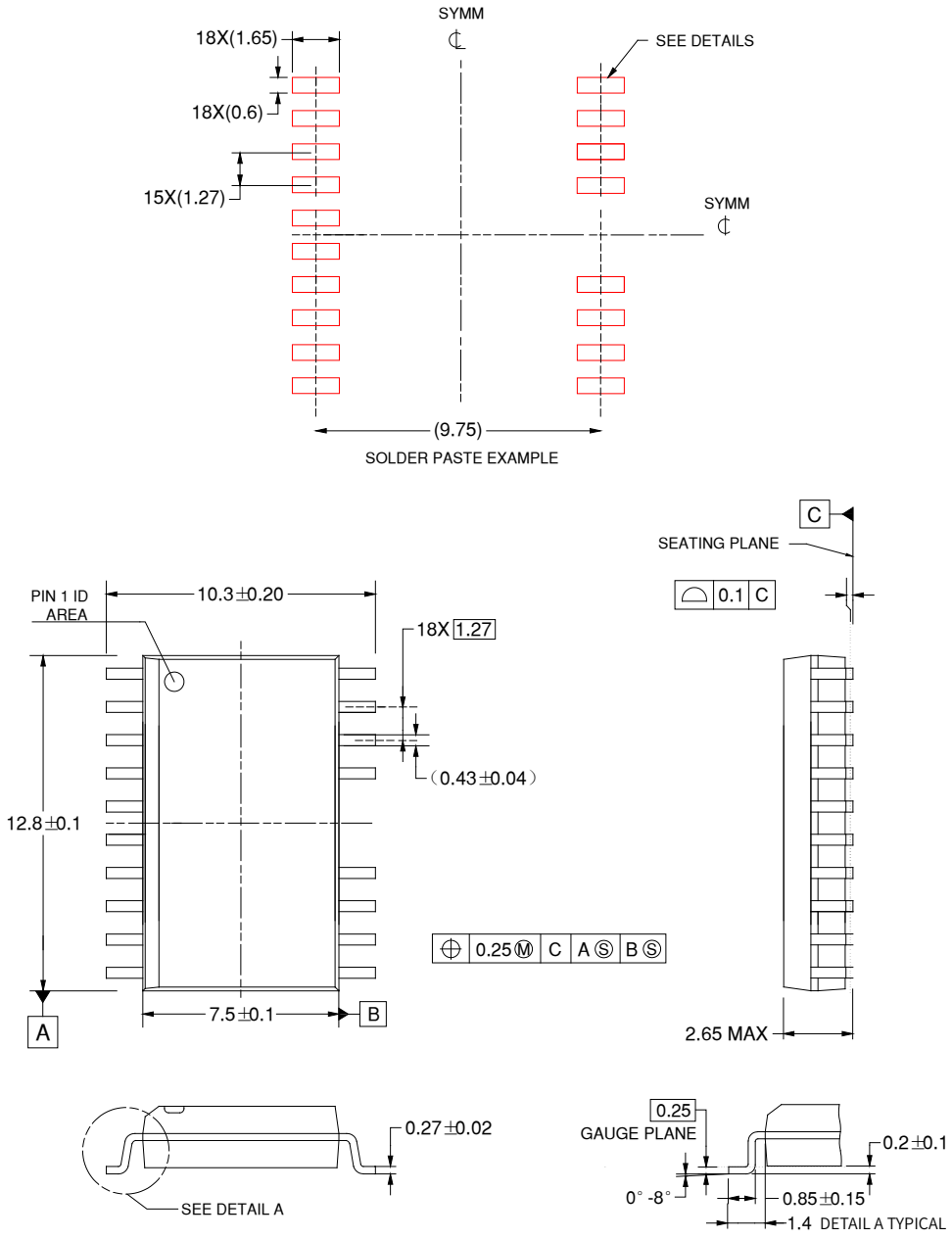


Figure 33. Dual-Supply Design

11.Packaging and Packing Information

11.1 Package Identifier



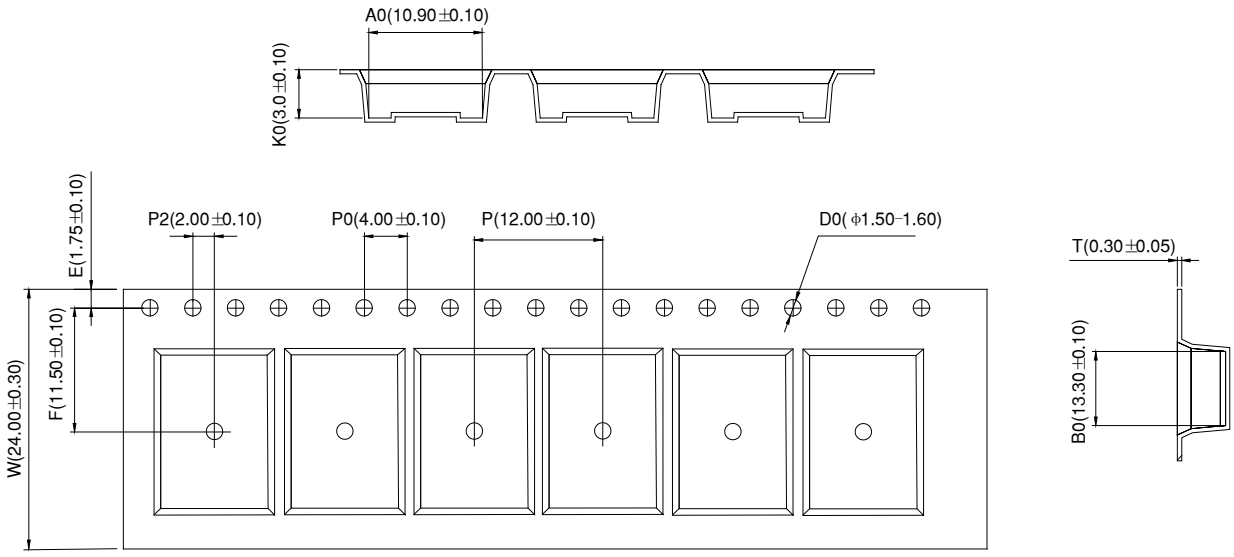
Note: 1) Legend unit: mm.

Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD.BASiC recommends that all integrated circuits be handled with appropriate precautions.Failure to observe proper handling and installation procedures can cause damage.

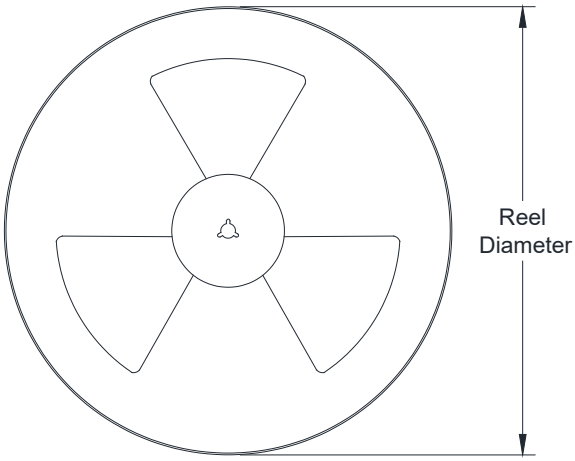
ESD damage can range from subtle performance degradation to complete device failure.Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.2 Packing Information



Note: 1) Legend unit: mm.

REEL DIMENSIONS



ITEM	FOOTPRINT
Reel Diameter	13 inches
Reel Width(W1)	24mm

12.Version Description

REVISION	NOTES	DATE
Rev.0.0	Released datasheet	24-Nov-2023
Rev.0.1	Primary Side Supply Voltage Value, Primary Side Power Supply Voltage Value, Package Infographic Update	25-Jan-2024
Rev.0.2	Add values for Thermal Information, Power Ratings, Safety-Limiting Values	31-Dec-2024
Rev.0.3	Modify the value I_{IH}, t_{PLH}, t_{PHL}, CMTI, VIOSM; Increase the value t_{DM}, DT	10-Apr-2025
Rev.0.4	Increase Typical Characteristics	09-Jun-2025
Rev.0.5	Update the minimum number of product packaging in the product information chapter	22-Jul-2025

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest BASiC Semiconductor Office

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