BTD5350x

Single-Channel Isolated Gate Driver

1.Features

- Isolation voltage up to 5000Vrms(SOW-8); 3000Vrms(SOP-8)
- Peak output current up to 10A
- Propagation delay 60ns
- Maximum switching frequency 1MHz
- Primary-side supply 3~18V
- Secondary-side supply up to 33V
- Primary-side and secondary-side power supply undervoltage lockout (UVLO)
- Compatible with 3.3V, 5V and 15V input
- Feature Options:
  Miller Clamp Options (BTD5350M)
  Split Outputs (BTD5350S)
  UVLO with respect to IGBT emitter (BTD5350E)
- 8-pin Package:
  SOP-8 with 4mm creepage
  SOW-8 with 8.5mm creepage
- Operating Temperature -40~125°C

2.Applications

- Motor drives
- EV chargers
- Telecommunication power supplies
- EV power supplies
- UPS
- String solar inverters

3.Description

BTD5350x is a family of single-channel, isolated gate driver with peak output current up to 10A, available in SOP-8 (narrow-body) or SOW-8 (wide-body) packages and supports isolation voltages up to 3000Vrms and 5000Vrms respectively. They can be used to drive IGBTs and Si/SiC MOSFETs. BTD5350x family offers 3 Feature Options:

BTD5350M provides Miller clamp function to prevent false turn-on caused by Miller current.

BTD5350S provides a split output with rise and fall time individually configurable.

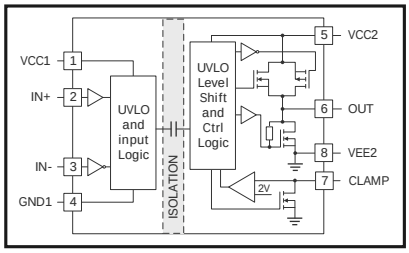
BTD5350E provides UVLO in positive power supply of secondary-side to ensure that power devices get sufficient gate turn-on voltage.

RoHS COMPLIANT

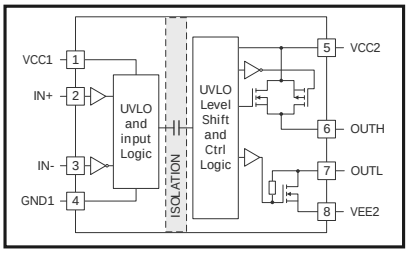
SOP-8

SOW-8

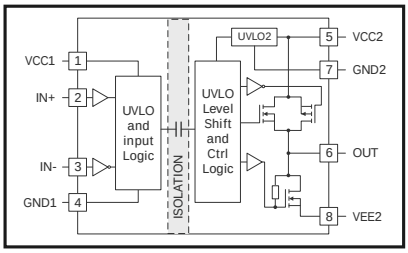
4.Functional Block Diagram



BTD5350M



BTD5350S



BTD5350E

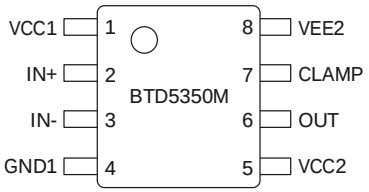
INDEX

5.Product Information

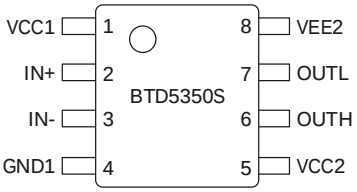
Part No.	Pin Configuration	Isolation Voltage	UVLO Threshold	Operating Temperature	Package	Package Material	Quantity	Marking
BTD5350MBPR	Miller-clamp	3000Vrms	8V	-40~125°C	SOP-8	Tape & Reel	2500pcs /Reel	BTD5350MB
BTD5350MCPR			11V					BTD5350MC
BTD5350MBWR		5000Vrms	8V		SOW-8		1000pcs /Reel	BTD5350MB
BTD5350MCWR			11V					BTD5350MC
BTD5350SBPR	Split output	3000Vrms	8V		SOP-8		2500pcs /Reel	BTD5350SB
BTD5350SCPR			11V					BTD5350SC
BTD5350SBWR		5000Vrms	8V		SOW-8		1000pcs /Reel	BTD5350SB
BTD5350SCWR			11V					BTD5350SC
BTD5350EBPR	UVLO with reference to GND2	3000Vrms	8V		SOP-8		2500pcs /Reel	BTD5350EB
BTD5350ECPR			11V					BTD5350EC
BTD5350EBWR		5000Vrms	8V		SOW-8		1000pcs /Reel	BTD5350EB
BTD5350ECWR			11V					BTD5350EC

6.Pin Configuration and Functions

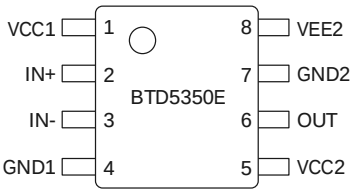
6.1 BTD5350M

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	VCC1	P	Input supply voltage	
2	IN+	I	Non-inverting gate signal input pin	
3	IN-	I	Inverting gate signal input pin	
4	GND1	G	Input ground	
5	VCC2	P	Positive output supply rail	
6	OUT	O	Gate-drive output	
7	CLAMP	I	Miller-clamp input	
8	VEE2	P	Negative output supply rail	
(1) P=Power, G=Ground, I=Input, O=Output				

6.2 BTD5350S

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	VCC1	P	Input supply voltage	
2	IN+	I	Non-inverting gate signal input pin	
3	IN-	I	Inverting gate signal input pin	
4	GND1	G	Input ground	
5	VCC2	P	Positive output supply rail	
6	OUTH	O	Gate-Drive pullup output pin	
7	OUTL	O	Gate-Drive pulldown output pin	
8	VEE2	P	Negative output supply rail	
(1) P=Power, G=Ground, I=Input, O=Output				

6.3 BTD5350E

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	VCC1	P	Input supply voltage	
2	IN+	I	Non-inverting gate signal input pin	
3	IN-	I	Inverting gate signal input pin	
4	GND1	G	Input ground	
5	VCC2	P	Positive output supply rail	
6	OUT	O	Gate-Drive pullup output pin	
7	GND2	G	Gate-Drive common pin	
8	VEE2	P	Negative output supply rail	
(1) P=Power, G=Ground, I=Input, O=Output				

7. Specification Parameters

7.1 Absolute Limits

SYMBOL	PARAMETER	MIN	MAX	UNIT
VCC1	Input bias pin supply voltage	-0.3	18	V
VCC2	Driver bias supply	-0.3	35	
-	V_{EE2} bipolar supply voltage for E version	-17.5	0.3	
-	Secondary side signal voltage	VEE2-0.3	VCC2+0.3	
V_{IN}	Primary side signal voltage	GND1-5	VCC1+0.3	
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-65	150	
T_L	Pin soldering temperature (10s)	-	300	
$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±3000		V
	Charge-device model (CDM), per ANSI/ESDA/JEDEC JS-002	±1500		
Note: These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability, and cause permanent damage to the device under severe conditions.				

7.2 Thermal Information

SYMBOL	PARAMETER	VALUE		UNIT
		SOP-8	SOW-8	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.7	91.4	°C /W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.4	35.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	43.0	73.8	
ψ_{JT}	Junction-to-top characterization parameter	57.3	51.0	
ψ_{JB}	Junction-to-board characterization parameter	65.7	47.7	

7.3 Power Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
SOP-8					
P_D	Maximum power dissipation on input and output	V_{CC1}=15V, V_{CC2}=15V, f=2.1MHz, 50% duty cycle square wave, 2.2nF load	-	1.43	W
P_{D1}	Maximum input power dissipation		-	0.05	
P_{D2}	Maximum output power dissipation		-	1.38	
SOW-8					
P_D	Maximum power dissipation on input and output	V_{CC1}=15V, V_{CC2}=15V, f=1.9MHz, 50% duty cycle square wave, 2.2nF load	-	1.36	W
P_{D1}	Maximum input power dissipation		-	0.05	
P_{D2}	Maximum output power dissipation		-	1.31	

7.4 Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC1}	Input supply voltage (VCC1–GND1)		3	15	V
V_{CC2}	Total supply voltage output side (VCC2–VEE2)	BTD5350xCx	13.2	33	
		BTD5350xBx	9.5	33	
V_{EE2}	Bipolar supply voltage for E version (VEE2–GND2)		-16	0	
T_A	Ambient temperature		-40	125	°C

7.5 Safety-Limiting Values

SYMBOL	PARAMETER	TEST CONDITIONS		SIDE	MIN	MAX	UNIT
SOP-8							
I_S	Safety output supply current	$R_{\theta JA}$=87.7°C /W, T_A=25°C , T_J= 150°C	VCC2=15V	Output side	-	92	mA
			VCC2=30V	Output side	-	46	
P_S	Safety supply power	$R_{\theta JA}$=87.7°C /W, T_A=25°C , T_J=150°C		INPUT	-	0.05	W
				Output side	-	1.38	
				TOTAL	-	1.43	
				-	-	150	
T_S	Safety temperature (1)				-	150	°C
SOW-8							
I_S	Safety output supply current	$R_{\theta JA}$=91.4°C /W, T_A=25°C , T_J=150°C	VCC2=15V	Output side	-	87	mA
			VCC2=30V	Output side	-	43.7	
P_S	Safety supply power	$R_{\theta JA}$=91.4°C /W, T_A=25°C , T_J=150°C		INPUT	-	0.05	W
				Output side	-	1.31	
				TOTAL	-	1.36	
				-	-	150	
T_S	Safety temperature (1)				-	150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

7.6 Electrical Characteristics

T_A=-40~125°C , V_{CC1}=3.3 or 5V, V_{CC2}=15V, C_L (1)=100pF.

Output pin: current towards outside of the chip is positive direction; Input pin: current towards inside of the chip is positive direction.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC1}	Input supply quiescent current	-	-	1.4	2.4	mA
I_{VCC2}	Output supply quiescent current	-	-	1.3	1.8	
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{ON1}	VCC1-GND1 Positive-going UVLO threshold voltage	-	-	2.6	2.8	V
V_{OFF1}	VCC1-GND1 Negative-going UVLO threshold voltage	-	2.4	2.5	-	
$V_{UV, HYS1}$	VCC1-GND1 UVLO threshold hysteresis	-	-	0.1	-	
UVLO THRESHOLDS						
V_{ON2}	VCC2-VEE2 Positive-going UVLO threshold voltage	BTD5350xCx	-	12	13	V
V_{OFF2}	VCC2-VEE2 Negative-going UVLO threshold voltage		10.3	11	-	
$V_{UV, HYS2}$	VCC2-VEE2 UVLO threshold voltage hysteresis		-	1	-	
V_{ON2}	VCC2-VEE2 Positive-going UVLO threshold voltage	BTD5350xBx	-	8.7	9.4	V
V_{OFF2}	VCC2-VEE2 Negative-going UVLO threshold voltage		7.3	8	-	
$V_{UV, HYS2}$	VCC2-VEE2 UVLO threshold voltage hysteresis		-	0.7	-	
LOGIC I/O						
V_{IH}	Input logic 1 (IN+, IN-)	-	-	0.55×V_{CC1}	0.7×V_{CC1}	V
V_{IL}	Input logic 0 (IN+, IN-)	-	0.35×V_{CC1}	0.45×V_{CC1}	-	
$V_{IN, HYS}$	Input Hysteresis voltage	-	-	0.1×V_{CC1}	-	
I_{IH}	High-level input leakage at IN+	IN+=V_{CC1}, V_{CC1}=5V	-	55	240	μA
I_{IL}	Low-level input leakage at IN-	IN-=GND1, V_{CC1}=5V	-240	-54	-	
		IN-=GND1-5V, V_{CC1}=5V	-310	-108	-	

(Continued)

GATE DRIVER STAGE						
I_{OH}	Peak source current	IN+=HIGH, IN-=LOW, C_L=470nF	-	10	-	A
I_{OL}	Peak sink current	IN+=LOW, IN-=HIGH, C_L=470nF	-	10	-	
V_{OH}	High level output voltage VCC2-OUT or VCC2-OUTH	I_{OUT}=+20mA IN+=HIGH, IN-=LOW	-	60	-	mV
V_{OL}	Low level output voltage OUT-VEE2 or OUTL-VEE2	I_{OUT}=-20mA IN+=LOW, IN-=HIGH	5	7	-	mV
MILLER CLAMP BTD5350Mx						
V_{clamp}	Low-level clamp voltage	I_{clamp}=20mA	-	7	10	mV
I_{clamp}	Low-level clamp current	V_{CLAMP}=VEEx+15V	5	10	-	A
$V_{clamp-TH}$	Clamping threshold voltage	-	-	2.2	-	V
SHORT-CIRCUIT CLAMPING						
$V_{CLP-OUT}$	Clamping voltage (OUT-VCC2 or OUTH-VCC2)	IN+=HIGH, IN–=LOW, t_{CLAMP}=10μs, I_{OUTH} or I_{OUT}=-500mA	-	1	1.3	V
	Clamping voltage (VEE2-OUT or VEE2-OUTL or VEE2-CLAMP)	IN+=LOW, IN–=HIGH, t_{CLAMP}=10μs, I_{CLAMP} or I_{OUTL}=500mA	-	1.5	-	
		IN+=LOW, IN–=HIGH, I_{CLAMP} or I_{OUTL}=20mA	-	0.9	1	
ACTIVE PULL-DOWN FUNCTION						
V_{OUTSD}	Active pulldown voltage on OUTL, CLAMP, OUT	I_{OUT}=-1A (sinking into OUT, OUTL or CLAMP pin), VCC2=left open	-	2.3	2.6	V
SWITCHING PARAMETERS						
t_{PLH}	Propagation delay, high	C_L=100pF	-	60	75	ns
t_{PHL}	Propagation delay, low	C_L=100pF	-	60	75	
t_r	Output-signal rise time	C_L=1nF	-	10	26	
t_f	Output-signal fall time	C_L=1nF	-	10	26	
t_{PWD}	Pulse width distortion $\lvert t_{PHL}-t_{PLH}\rvert$	C_L=100pF	-	1	20	
t_{sk} 2)	Part-to-part skew	C_L=100pF	-	1	25	
$t_{UVLO1-rec}$	Undervoltage lockout recovery delay time — Input side	VCC1	-	50	-	μs
$t_{UVLO2-rec}$	Undervoltage lockout recovery delay time — Output side	VCC2	-	50	-	
CMTI	Common-mode transient immunity	INx tied to GND or VCC1, V_{CM}=1500V	150	-	-	kV/μs

Note: 1. C_L: Load capacitance from output pin OUTx to VEE2 or GND2.
2. t_{sk} is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads guaranteed by characterization.

7.7 Insulation Specifications

7.7.1 SOP-8 Safety Parameters

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
CLR	External Clearance	Shortest pin-to-pin distance through air	⩾ 4	mm
CPG	External Creepage	Shortest pin-to-pin distance across the package surface	⩾ 4	
DTI	Distance through insulation	-	⩾ 17	μm
CTI	Comparative tracking index	DIN EN 60112	⩾ 600	V
-	Material Group	IEC 60664-1	I	-
-	Overvoltage category per IEC 60664-1	Rated mains voltage ⩽ 150Vrms	I-IV	
		Rated mains voltage ⩽ 300Vrms	I- III	
DIN VDE V0884-11				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	990	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	700	Vrms
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST}=V_{IOTM}=V_{ISO}$, t=60s (qualification) ; $V_{TEST}=V_{IOTM}=1.2\times V_{ISO}$, t=1s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 62368-1, 1.2/50-μs waveform, $V_{TEST}=1.3\times V_{IOSM}$ (qualification)	4242	
q_{pd}	Apparent charge	Method a: After I/O safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini}=60s, $V_{pd(m)}=1.2\times V_{IORM}$, t_m=10s	⩽ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s, $V_{pd(m)}=1.2\times V_{IORM}$, t_m=10s	⩽ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini}=1.2\times V_{IOTM}$, t_{ini}=1s, $V_{pd(m)}=1.5\times V_{IORM}$, t_m=1s	⩽ 5	
C_{IO}	Barrier capacitance, input to output	$V_{IO}=0.4\times\sin(2\pi ft)$, f=1MHz	1.2	pF
R_{IO}	Isolation resistance, input to output	Test voltage of 500V, T_A=25°C	$>10^{12}$	Ω
		Test voltage of 500V, 100°C⩽ T_A ⩽ 125°C	$>10^{11}$	
		Test voltage of 500V, T_S=150°C	$>10^{9}$	
-	Pollution degree	-	2	-
-	Climatic category	-	40/125/21	-
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST}=V_{ISO}$, t=60s (qualification) ; $V_{TEST}=1.2\times V_{ISO}$, t=1s (100% production)	3000	Vrms

7.7.2 SOW-8 Safety Parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	UNIT
CLR	External Clearance	Shortest pin-to-pin distance through air	⩾ 8.5	mm
CPG	External Creepage	Shortest pin-to-pin distance across the package surface	⩾ 8.5	
DTI	Distance through insulation	-	⩾ 17	μm
CTI	Comparative tracking index	DIN EN 60112	⩾ 600	V
-	Material Group	IEC 60664-1	I	-
-	Overvoltage category per IEC 60664-1	Rated mains voltage ⩽ 600Vrms	I-III	
		Rated mains voltage ⩽ 1000Vrms	I-II	
DIN V VDE 0884–11				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	1500	Vrms
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST}=V_{IOTM}=V_{ISO}$, t=60s (qualification) ; $V_{TEST}=V_{IOTM}=1.2\times V_{ISO}$, t=1s (100% production)	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 62368-1, 1.2/50-μs waveform, $V_{TEST}=1.6\times V_{IOSM}$ (qualification)	6250	
q_{pd}	Apparent charge	Method a: After I/O safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini}=60s, $V_{pd(m)}=1.2\times V_{IORM}$, t_m=10s	⩽ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s, $V_{pd(m)}=1.6\times V_{IORM}$, t_m=10s	⩽ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini}=1.2\times V_{IOTM}$, t_{ini}=1s, $V_{pd(m)}=1.875\times V_{IORM}$, t_m=1s	⩽ 5	
C_{IO}	Barrier capacitance, input to output	$V_{IO}=0.4\times\sin(2\pi ft)$, f=1MHz	1.2	pF
R_{IO}	Isolation resistance, input to output	Test voltage of 500V, T_A=25°C	$>10^{12}$	Ω
		Test voltage of 500V, 100°C⩽ T_A ⩽ 125°C	$>10^{11}$	
		Test voltage of 500V, T_S=150°C	$>10^{9}$	
-	Pollution degree	-	2	-
-	Climatic category	-	40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST}=V_{ISO}$, t=60s (qualification) ; $V_{TEST}=1.2\times V_{ISO}$, t=1s (100% production)	5000	Vrms

7.7.3 SOW-8 Packing Safety-Related Certifications

UL	VDE	CQC
Recognized under UL 1577 Component Recognition Program	Plan to certify according to DIN V VDE V0884-11:2017-01 and DIN EN 61010-1	Plan to certify according to GB 4943.1-2011
Single protection, 5000 V_{RMS}	Reinforced Insulation Maximum Transient isolation Overvoltage, 7000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 2121 V_{PK}; Maximum Surge Isolation Voltage, 6250 V_{PK}	Reinforced Insulation, Altitude ⩽ 5000 m, Tropical Climate
File Number：E537161	Certification planned	Certification planned

8.Parameter Testing

8.1 Propagation Delay

The method for measuring the rise time (t_r) and fall time (t_f) : the propagation delay OUTH and OUTL for non-inverting input (see Figure 1); the propagation delay for inverting input (see Figure 2).

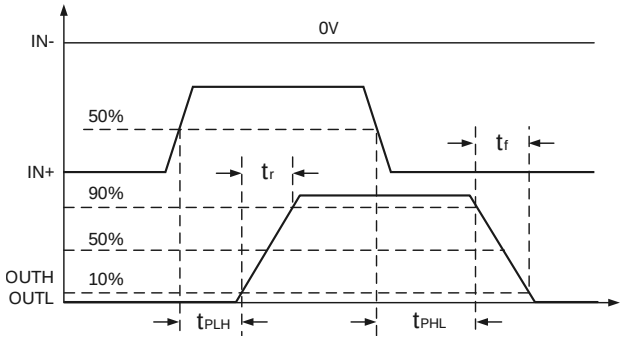


Figure 1. Input and Output Propagation Delay (Non-Inverting Configuration)

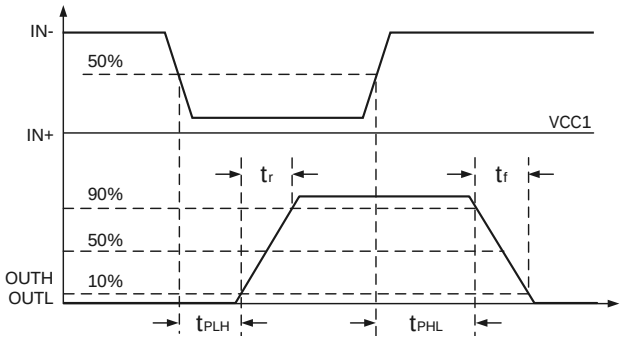


Figure 2. Input and Output Propagation Delay (Inverting Configuration)

8.2 CMTI

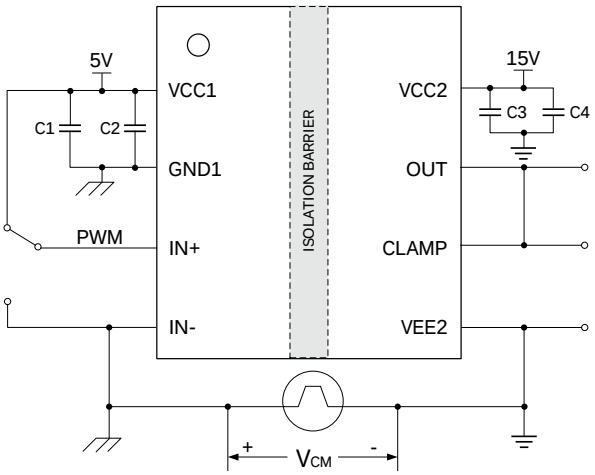


Figure 3. CMTI Test Circuit for BTD5350Mx

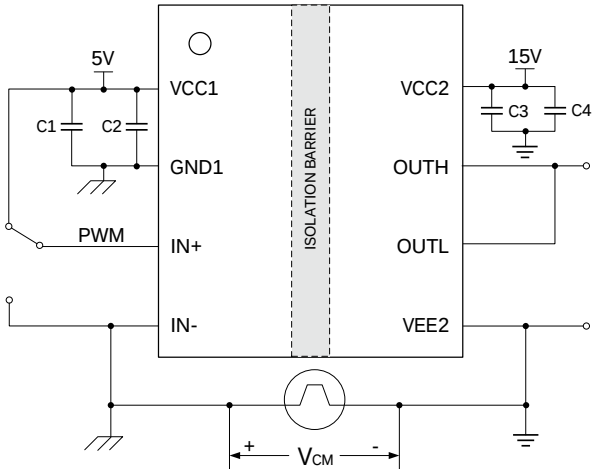


Figure 4. CMTI Test Circuit for BTD5350Sx

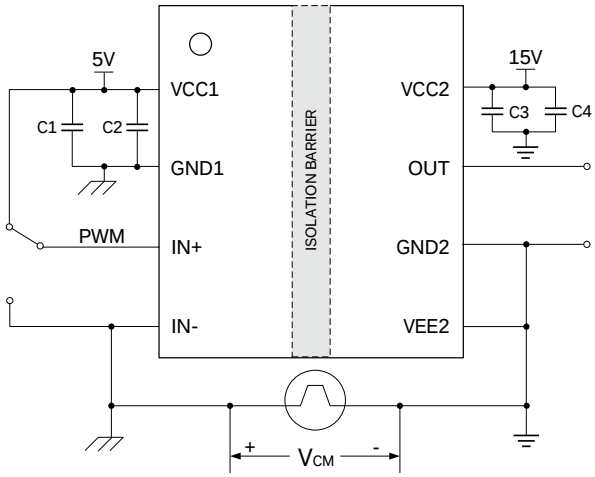


Figure 5. CMTI Test Circuit for BTD5350Ex

8.3 Typical Characteristics

T_A=-40~125℃ , V_{CC1}=3.3V or 5V, V_{CC2}=15V, C_L=100pF. unless otherwise indicated.

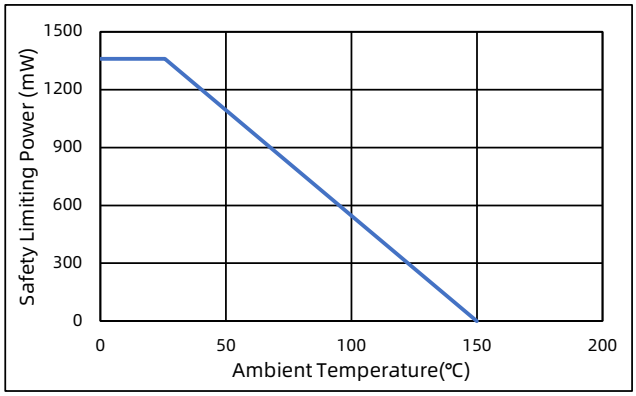


Figure 6. Temperature derating curve of safe power

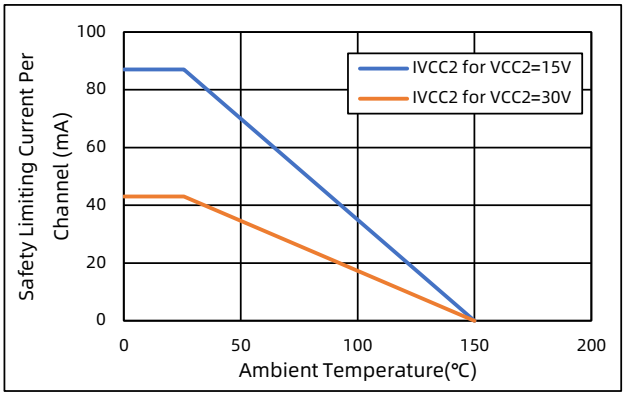


Figure 7. Temperature derating curve of safety current

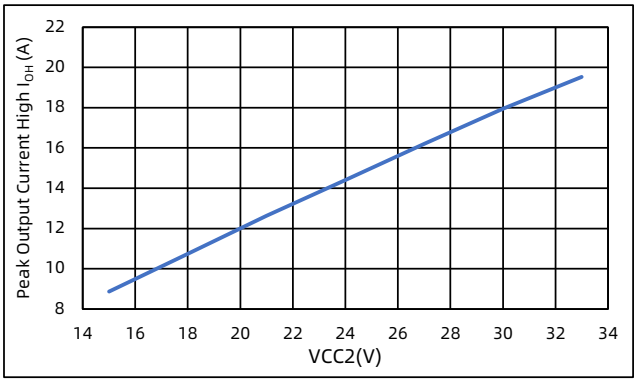


Figure 8. Output high level drive current vs. Output voltage (C_L=150nF)

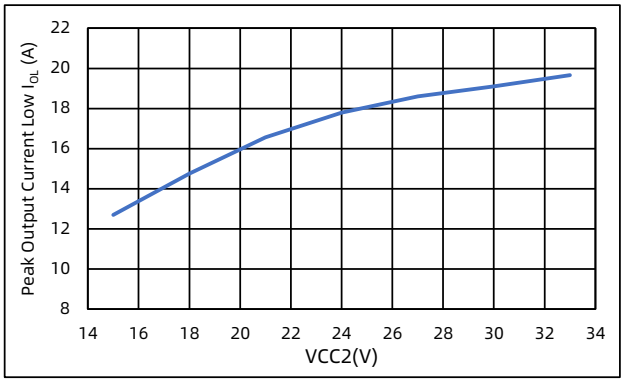


Figure 9. Output low level drive current vs. Output voltage (C_L=150nF)

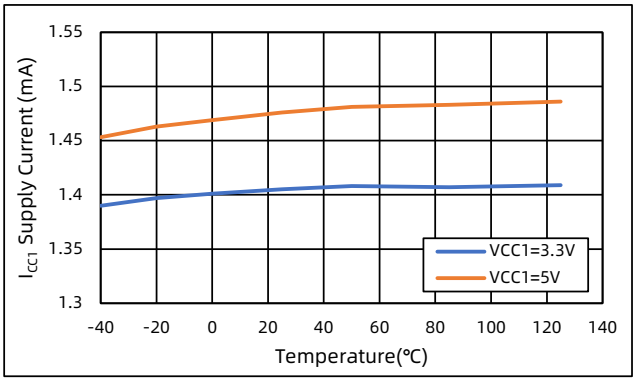


Figure 10. I_{CC1} power supply current vs. Temperature (IN+=L, IN-=H)

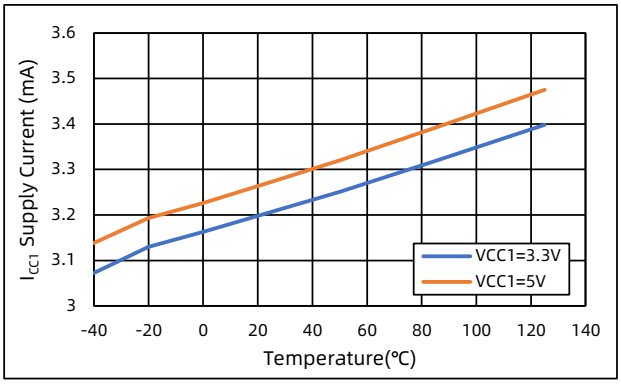


Figure 11. I_{CC1} power supply current vs. Temperature (IN+=H, IN-=L)

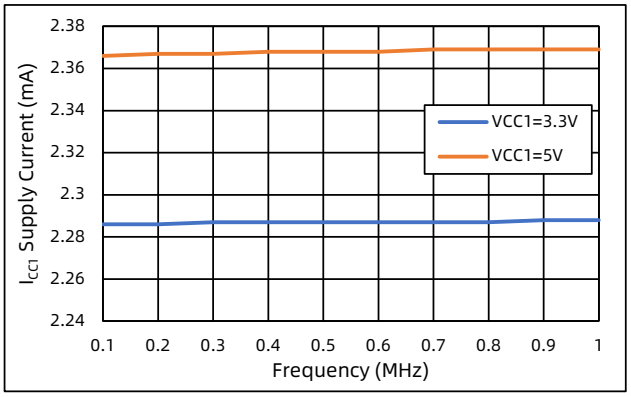


Figure 12. I_{CC1} power supply current vs. Input frequency

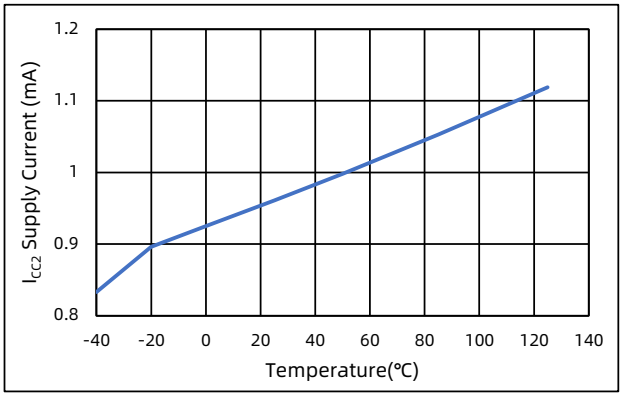


Figure 13. I_{CC2} power supply current vs. Temperature (IN+=L, IN-=H)

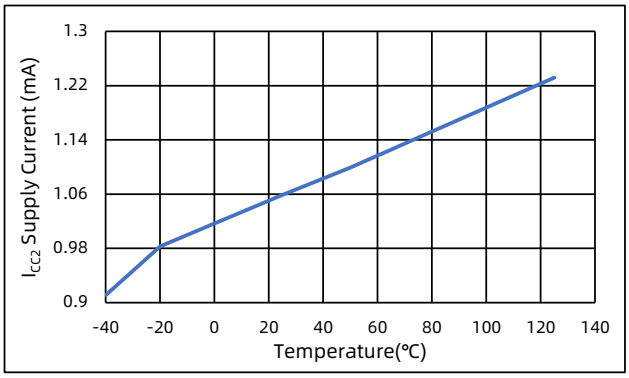


Figure 14. I_{CC2} power supply current vs. Temperature (IN+=H, IN-=L)

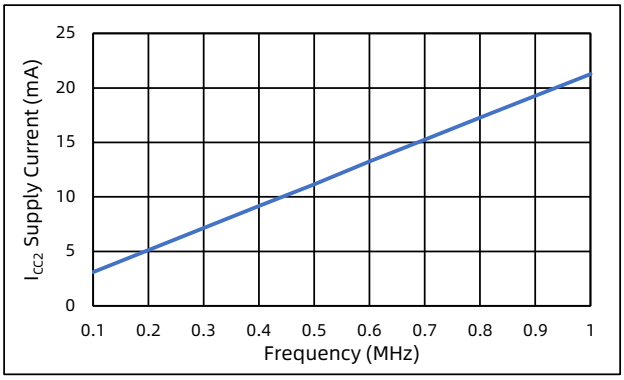


Figure 15. I_{CC2} power supply current vs. Input frequency

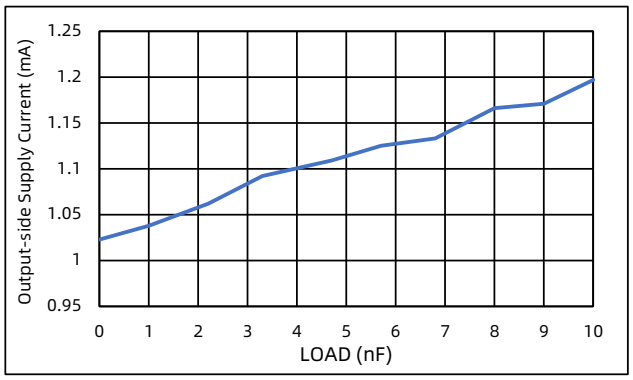


Figure 16. I_{CC2} power supply current vs. Load capacitance (f=1kHz)

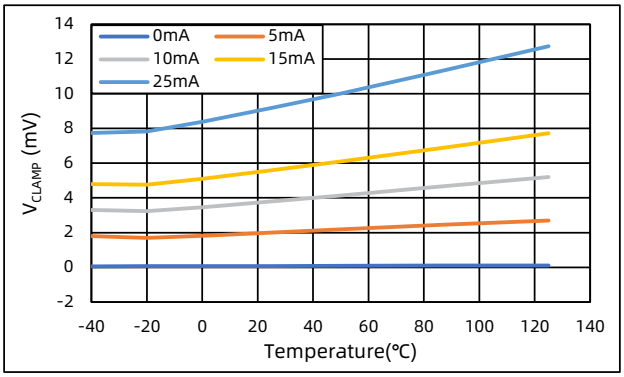


Figure 17. V_{CLAMP} vs. Temperature

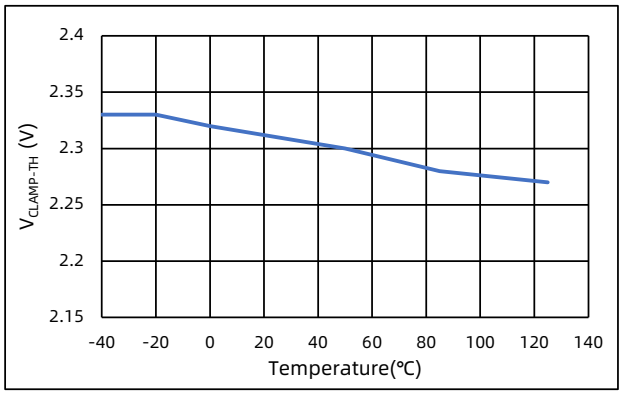


Figure 18. $V_{CLAMP-TH}$ vs. Temperature

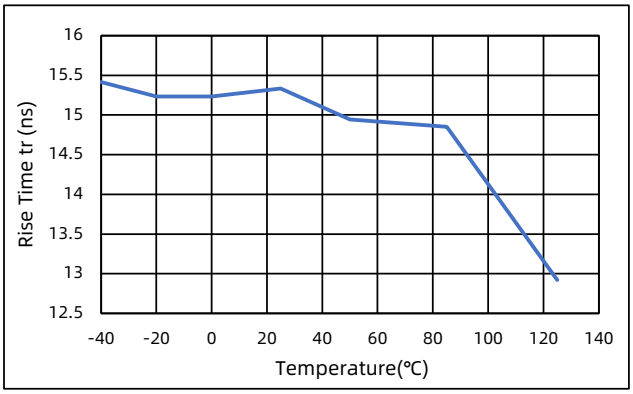


Figure 19. Rise time vs. Temperature

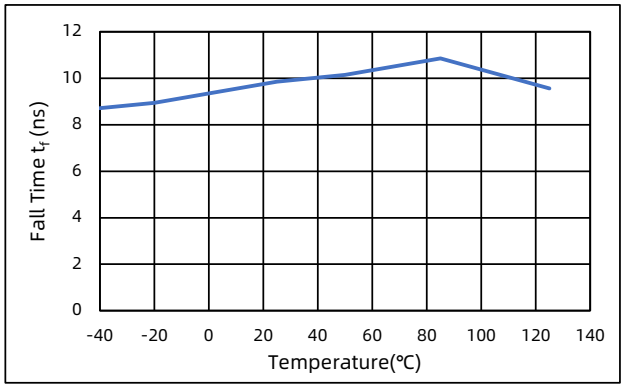


Figure 20. Fall time vs. Temperature

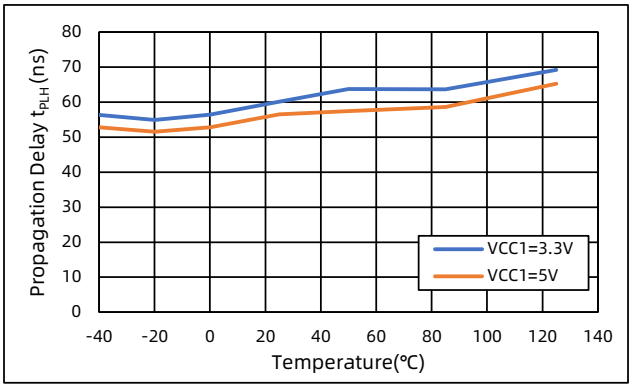


Figure 21. Transmission delay t_{PLH} vs. Temperature (C_L=1nF)

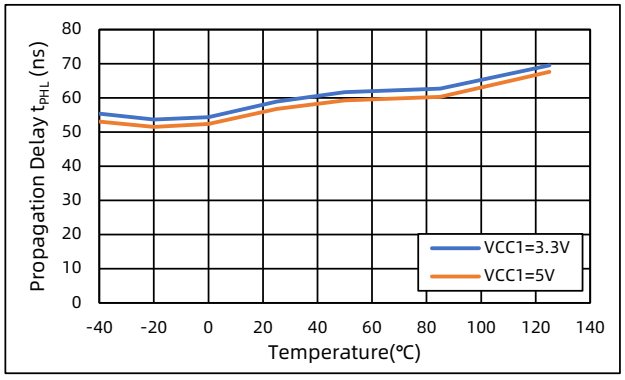


Figure 22. Propagation delay t_{PHL} vs. Temperature (C_L=1nF)

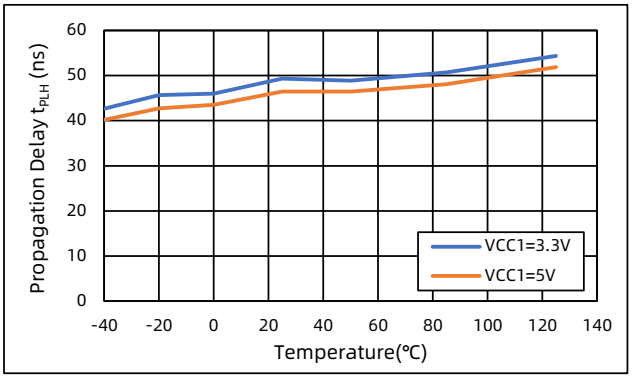


Figure 23. Propagation delay t_{PHL} vs. Temperature (C_L=100pF)

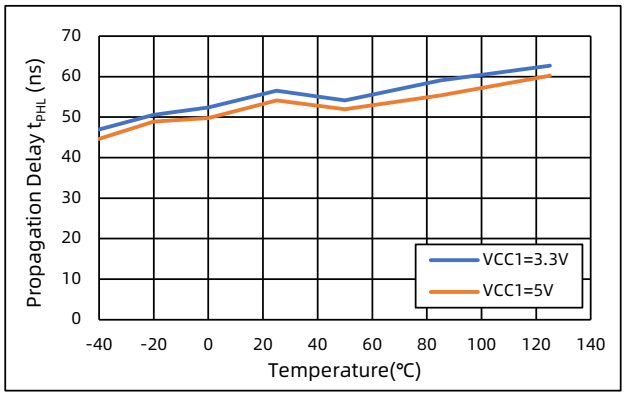


Figure 24. Propagation delay t_{PHL} vs. Temperature (C_L=100pF)

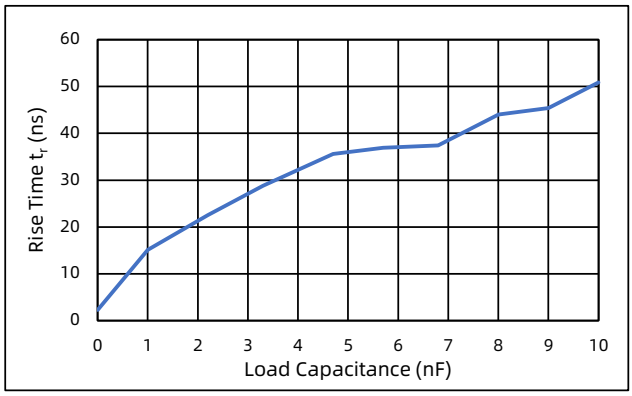


Figure 25. Rise time vs. Load capacitance

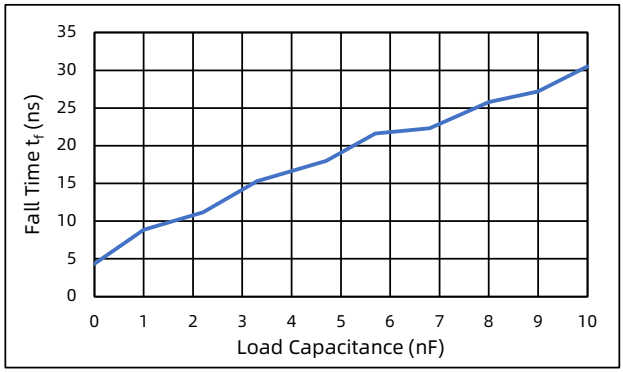


Figure 26. Fall time vs. Load capacitance

9.Function Description

9.1 Isolation Design Description

The isolation inside the BTD5350x series is implemented with high voltage SiO_2 based capacitors. There is a capacitor on each of the primary-side and secondary-side to enhance insulation. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data. The primary-side transmits a high-frequency carrier to represent one digital state, and sends no signal to represent the other digital state. On the secondary side, the receiver demodulates the signal and produces output for control. One can also add special anti-jamming circuit on the primary /secondary sides to enhance the CMTI performance and minimize the radiate emissions (see Figure 27, 28).

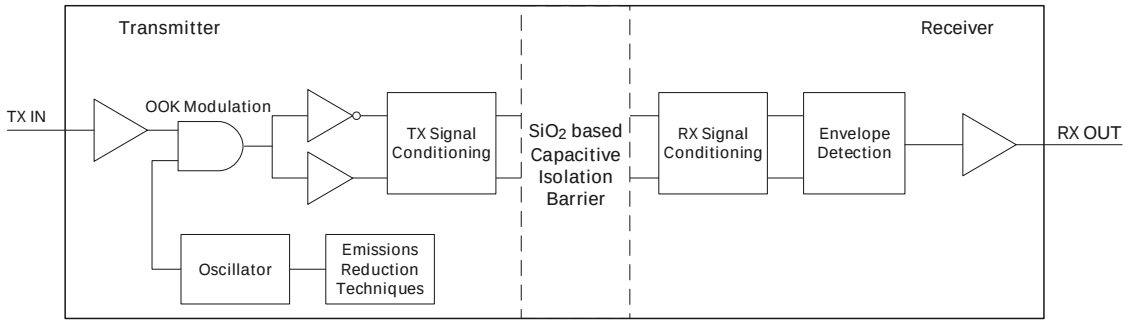


Figure 27. Conceptual Block Diagram of a Capacitive Data Channel

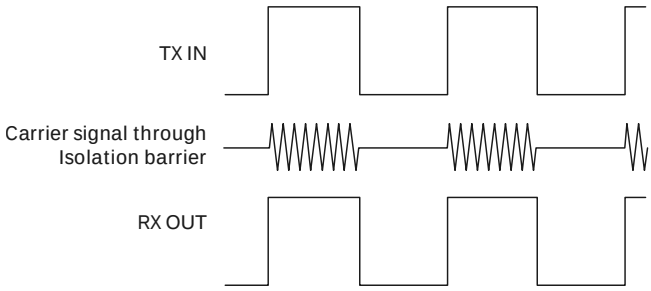


Figure 28. OOK Based Modulation Scheme

9.2 Input Stage Characteristics

With input pins and secondary side completely isolated, BTD5350x is designed to be CMOS-compatible. It supports 3.3V, 5V and 15V level input, making the chip easy to accept control of multiple logic levels. It also has a internal integrated filter circuit with 0.1* VCC1 hysteresis for improving noise immunity of the input stage. The IN+ input port has a 128kΩ pull-down resistor to force it grounding, the IN- input port has a 128kΩ pull-up resistor to make it go high to the power supply, which can ensure that the output ports are in OFF state when input ports are left open. However, in order to configure the initial power-on state of the driver IC, BASiC still recommends adding externally an appropriate pull-up or pull-down resistor to the input.

9.3 Output Booster Characteristics

The BTD5350x has a rail-to-rail push stage output. The pull-up structure of the output stage consists of a P-channel MOSFET and an N-channel MOSFET connected in parallel. At turn-on, N-channel MOSFET provides high current driving capability. P-channel MOSFET provides a small steady-state conduction voltage drop during steady conduction. The pull-down structure is implemented using an N-channel MOSFET. A 1MΩ resistor is connected in parallel between the drain and gate of the MOSFET to effectively clamp the gate voltage of the power device in the event of a loss of power on the chip to prevent the occurrence of partial turn-on. However, in order to ensure reliable shutdown of the power device, BASiC recommends that appropriate pull-down resistor be added to the gate.

In order to prevent the output port voltage from overvoltage/overcurrent damage when the positive secondary-side power supply voltage VCC2 becomes lower than the negative secondary-side power supply voltage VEE2, due to gate oscillation on output terminals, the 5350M version is designed with a Miller clamp on the output port to effectively suppress oscillations. However, to ensure the normal operation of the drive circuit, BASiC recommends to use Schottky diodes at the gate to clamp the positive and negative power supplies respectively.

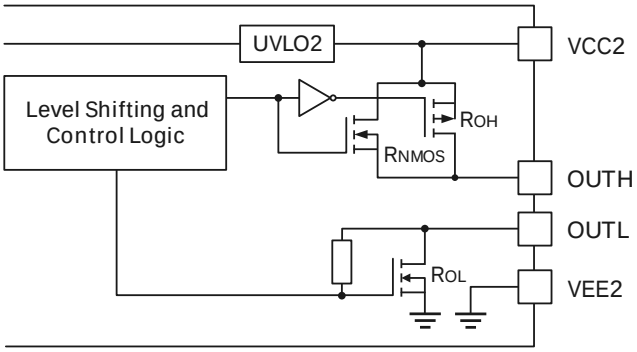


Figure 29. Output Stage

9.4 Protection Functions

9.4.1 Undervoltage Lockout

The BTD5350x has undervoltage lockout (UVLO) function on the primary-side power supply and the secondary-side total supply voltage to prevent the gate drive voltage from being insufficient. When the supply voltage drops below UVLO threshold, the ASIC turns off the output to protect the power devices. When the supply voltage reaches the positive-going negative-going threshold, the ASIC resumes the output. To prevent repeated action near the UVLO threshold, the ASIC is configured with hysteresis. In order to avoid the uncertainty of the output state after power-on, the ASIC first enters an UVLO state after power-on, keeps the output off until the supply voltage is established and then starts normal operation (see Figure 30).

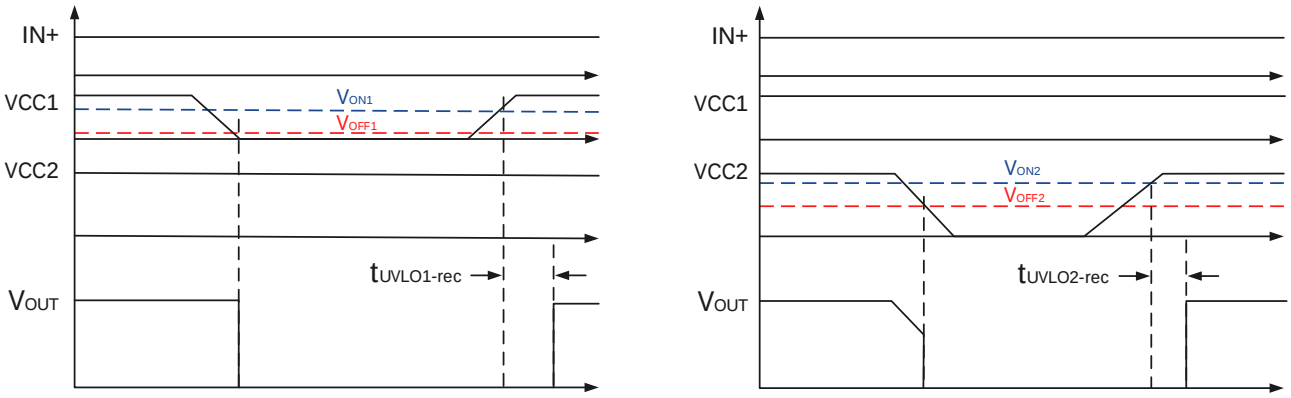


Figure 30. UVLO Functions

9.4.2 Miller Clamp

The active Miller clamp function is used to prevent the power devices from false turn-on of the power switched cause by the Miller current. A low impedance path is added between the gate terminal and ground (VEE2) to sink the Miller current. The Miller clamp function clamps the gate voltage of the power device to less than 2V when the output is in the off state.

9.4.3 Short-Circuit Clamping

In short-circuit conditions, the gate voltage of the power devices tend to rise, so the short-circuit clamping function is used to clamp its gate voltage. The short-circuit clamping function helps protect the IGBT or MOSFET gates from overvoltage breakdown or degradation. The short circuit clamping function is implemented by adding a diode between the OUT, OUTL or CLAMP pins and the VCC2 pins inside the driver. The internal diode can carry a current up to 500mA for 10μs or a continuous current of 20mA. Use external Schottky diodes to improve current conduction capability as needed.

9.4.4 Active Pull-Down

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the VCC2. This feature prevents false IGBT and MOSFET turn-on on the OUT, OUTL and CLAMP pins by clamping the output to approximately 2V.

9.5 ESD Structure

The figure below shows the ESD-protected diode configuration of the input and output pins.

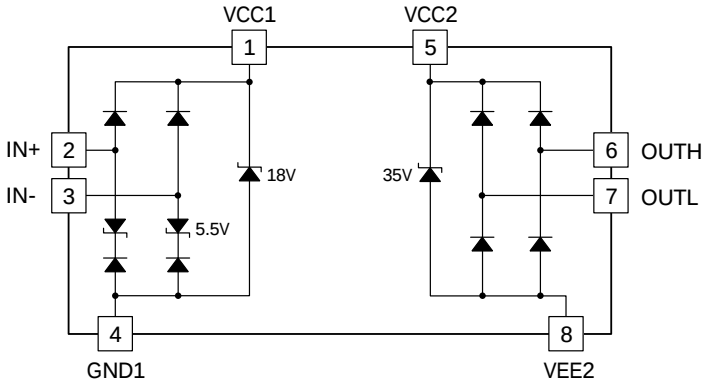


Figure 31. ESD Structure Diagram

9.6 Truth Table

BTD5350M and BTD5350E

IN+	IN-	VCC1	VCC2	OUT
X	X	<UVLO	X	L
X	X	X	<UVLO	L
H	L	>UVLO	>UVLO	H
H	H	>UVLO	>UVLO	L
L	L	>UVLO	>UVLO	L
L	H	>UVLO	>UVLO	L

BTD5350S

IN+	IN-	VCC1	VCC2	OUTH	OUTL
X	X	<UVLO	X	Hi-Z	L
X	X	X	<UVLO	Hi-Z	L
H	L	>UVLO	>UVLO	H	Hi-Z
H	H	>UVLO	>UVLO	Hi-Z	L
L	L	>UVLO	>UVLO	Hi-Z	L
L	H	>UVLO	>UVLO	Hi-Z	L

10.Applications

The following sections introduce the basic typical application of BASiC driver ICs, which is for reference only. In practical application, users need to verify and test its applicability according to their own design requirements to confirm the system functions.

10.1 Typical Applications

BASiC recommends that customers add a RC filter with a small time constant at the input port to filter out high-frequency interference without adding a large delay. It is recommended that the resistance value should be be-tween 0 and 100Ω and the capacitance should be less than 1000pF. When setting this parameter, the influence between high frequency interference and delay needs to be taken into account.

To ensure the supply stability, BASiC recommends to add appropriate blocking capacitor between the power supply and ground. It is recommended to parallel a 1uF+ 0.1uF capacitor between VCC1-GND1, and a 10uF+ 0.22uF capacitor between VCC2-VEE2 (Figure 32,33,34).

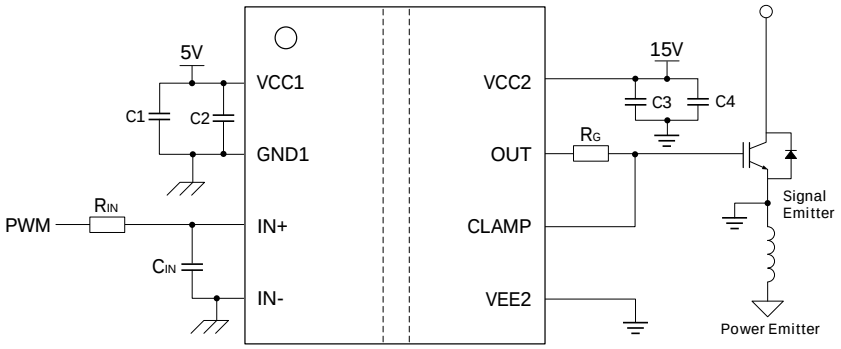


Figure 32. Typical Application Circuit for BTD5350M

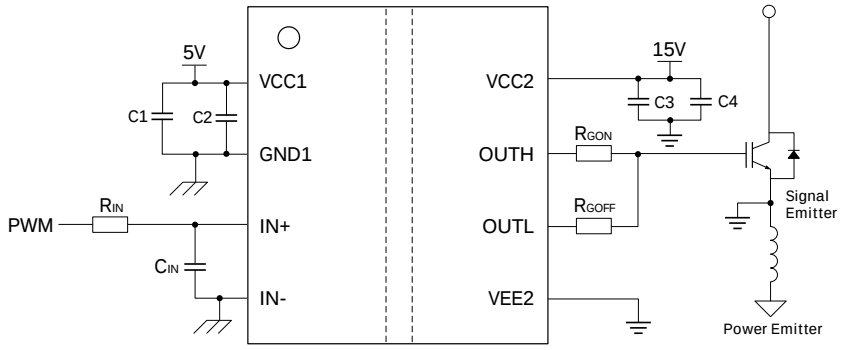


Figure 33. Typical Application Circuit for BTD5350S

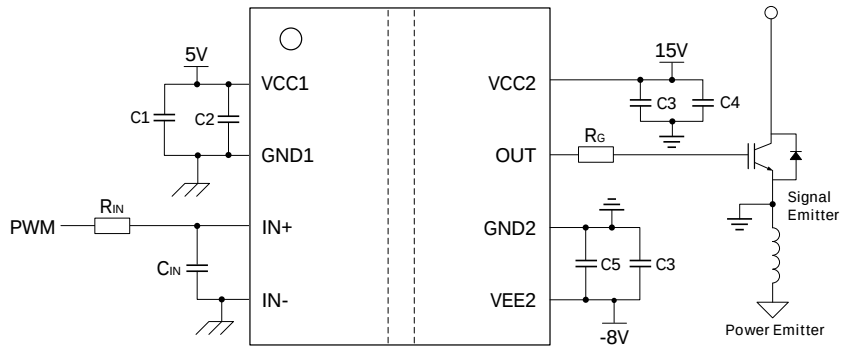


Figure 34. Typical Application Circuit for BTD5350E

10.2 Recommended Design Of Secondary Side Supply

In order to avoid false turn-on of the gate of the power device due to interference, it is recommended that customers add a negative power supply when designing the driving output. It is recommended to use the following two methods to generate the negative supply: use a regulator to generate stable negative voltage (see Figure 35); or use both positive and negative supplies (see Figure 36).

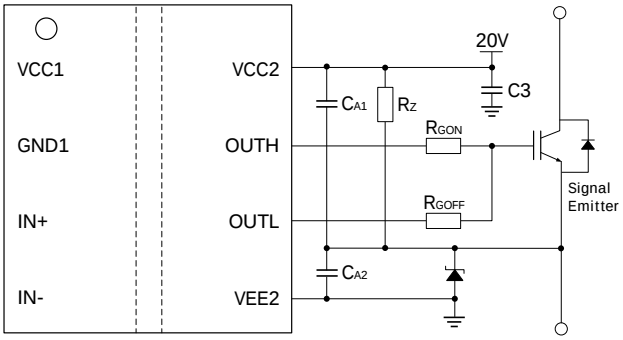


Figure 35. Voltage Regulator Design

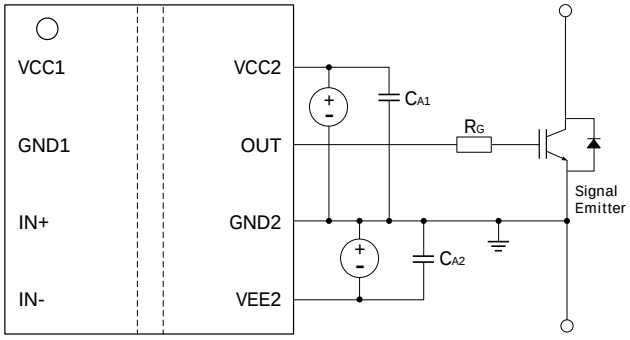
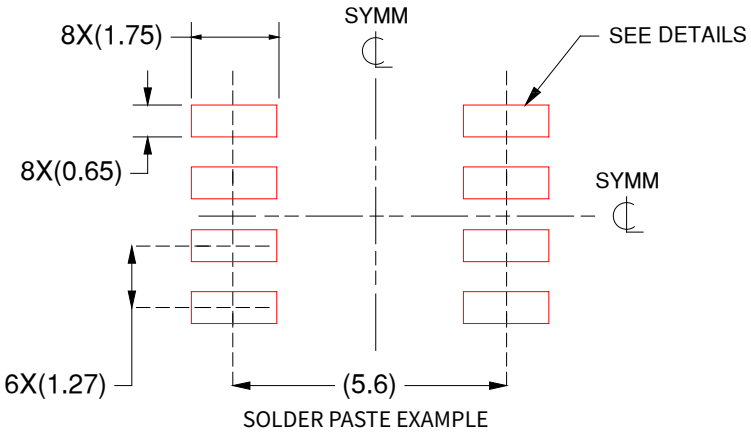


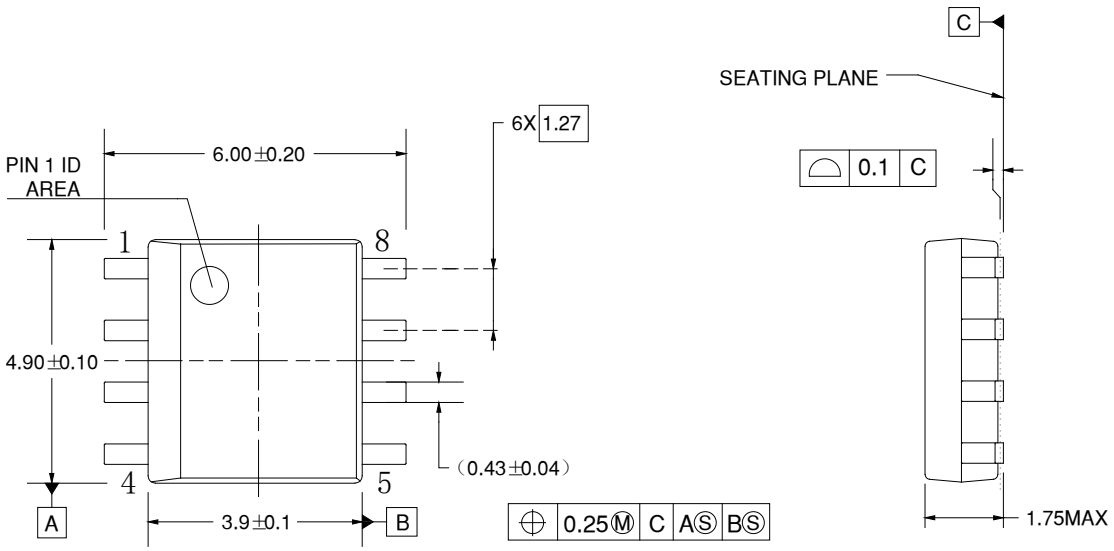
Figure 36. Dual-Supply Design

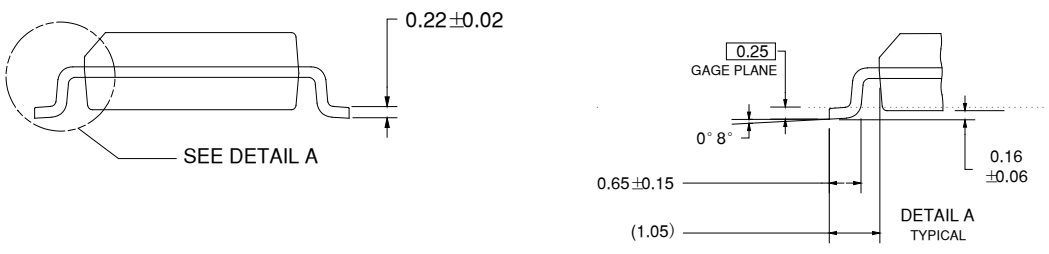
11.Packaging and Packing Information

11.1 Package Identifier

11.1.1 SOP-8 Package Identifier

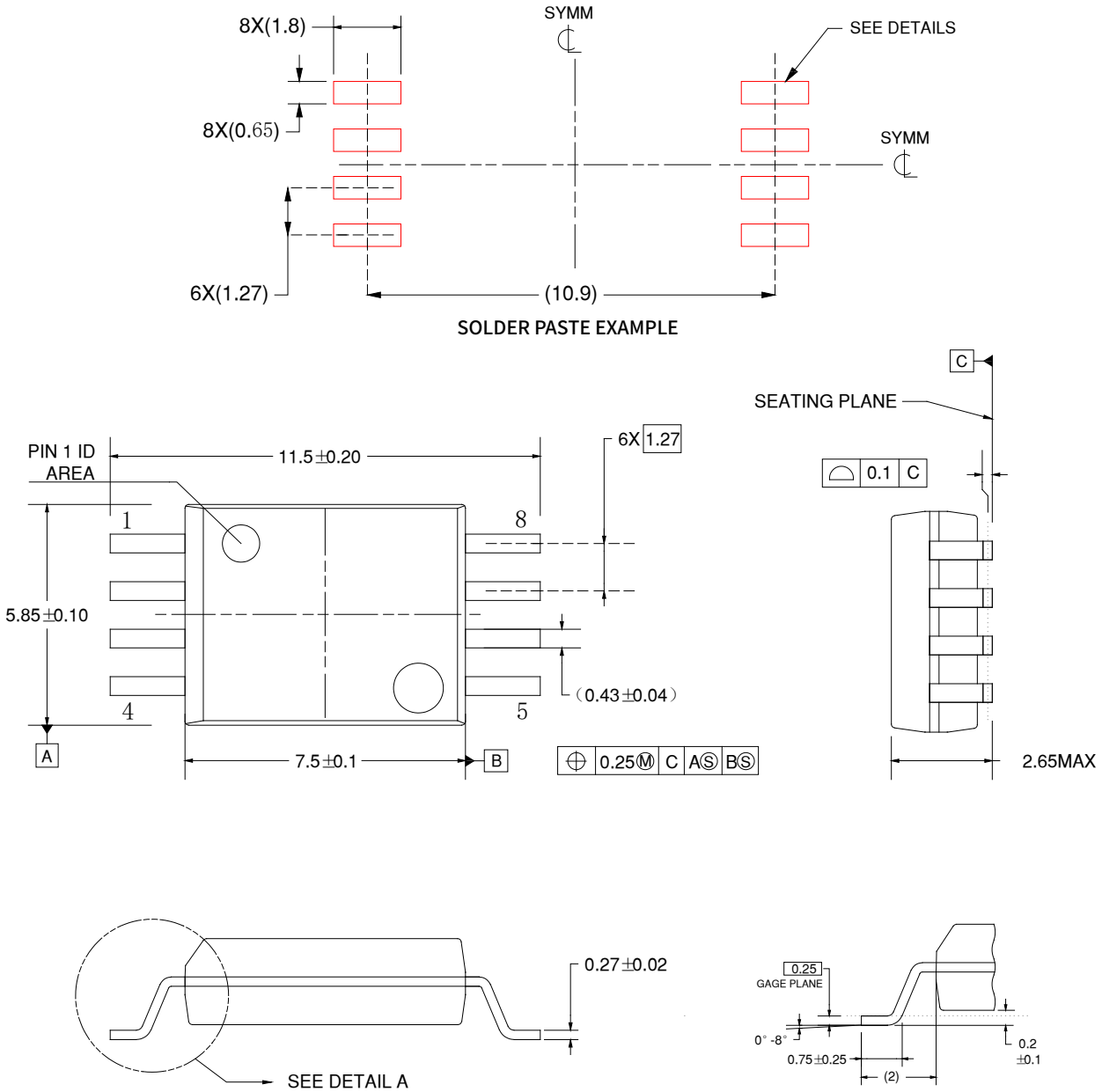






Note: 1) Legend unit: mm.

11.1.2 SOW-8 Package Identifier



Note: 1) Legend unit: mm.

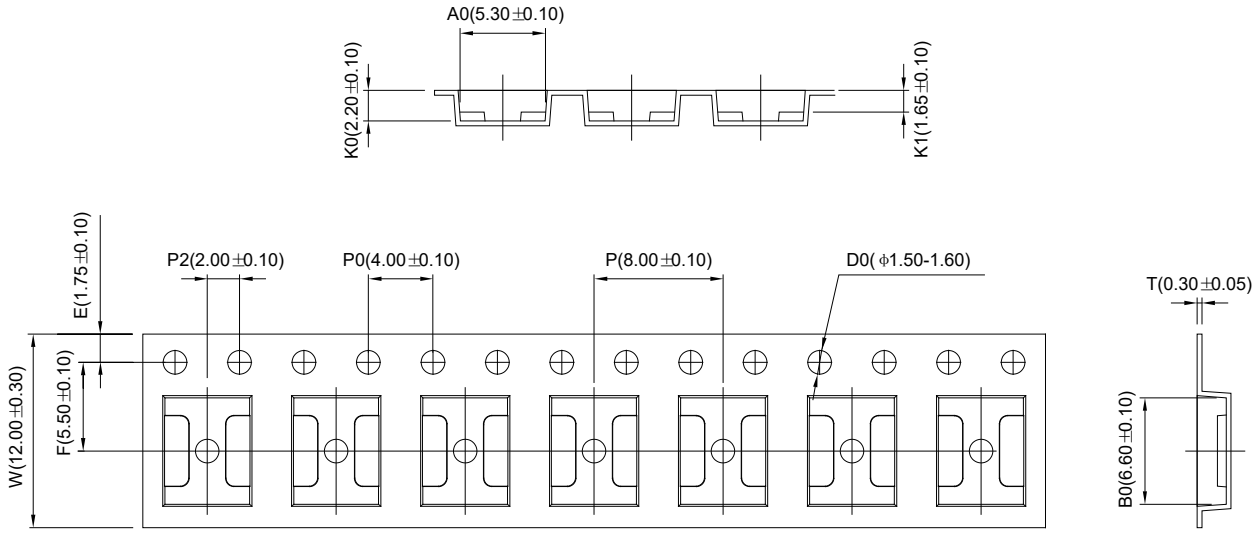
Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD.BASiC recommends that all integrated circuits be handled with appropriate precautions.Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure.Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

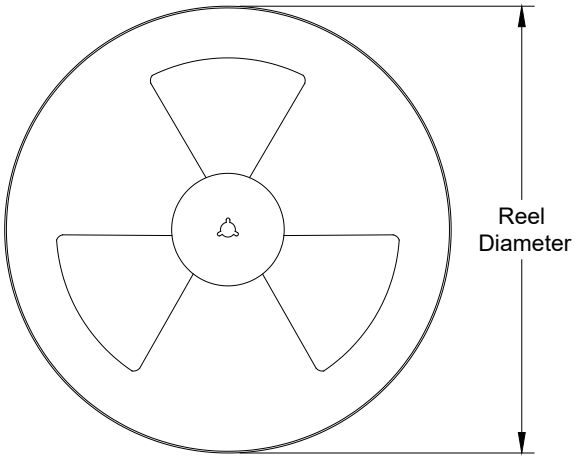
11.2 Packing Information

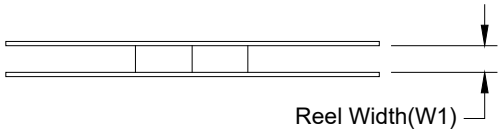
11.2.1 SOP-8 Packing Information



Note: 1) Legend unit: mm.

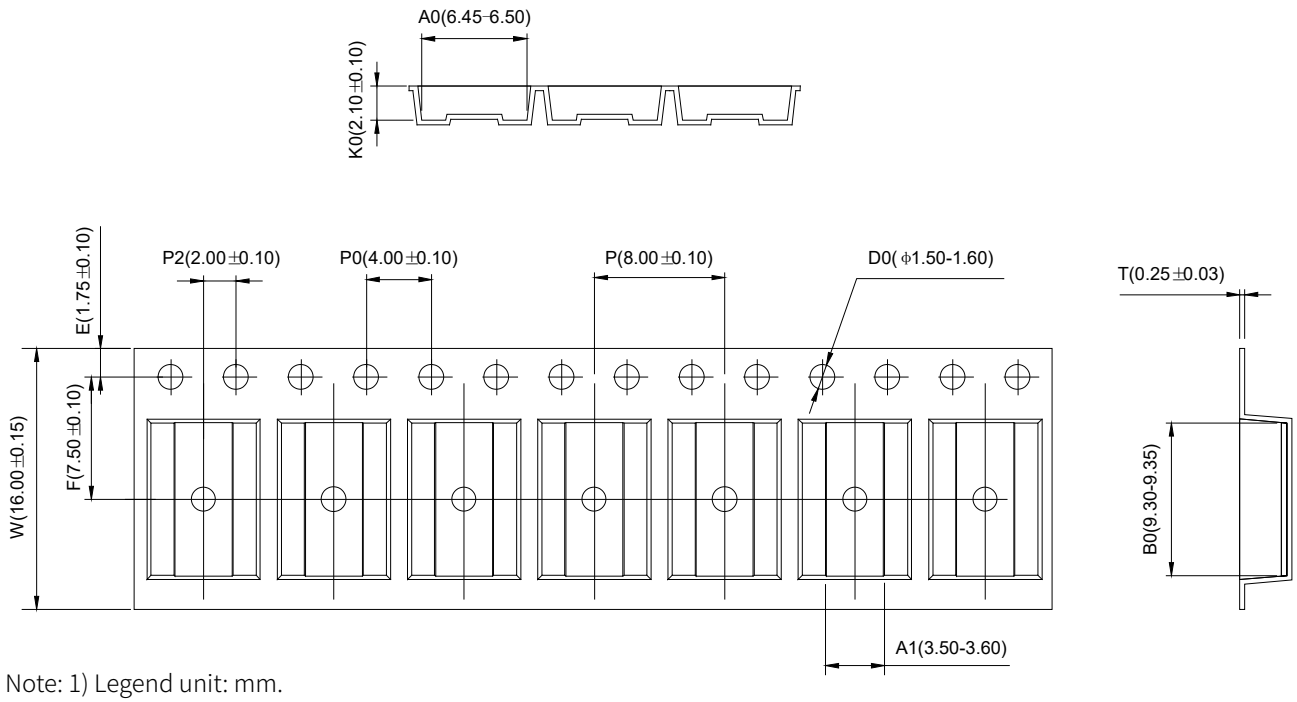
REEL DIMENSIONS





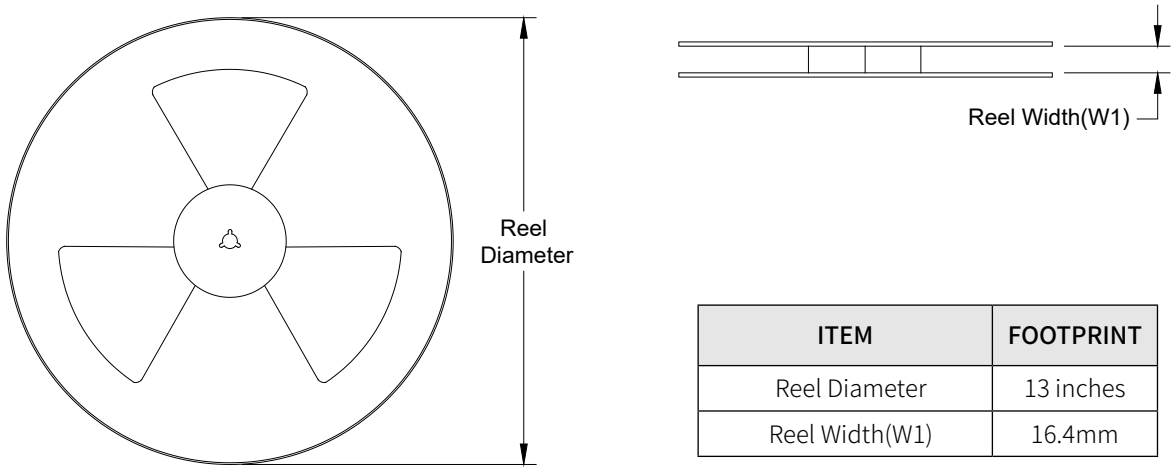
ITEM	FOOTPRINT
Reel Diameter	13 inches
Reel Width(W1)	12.4mm

11.2.2 SOW-8 Packing Information



Note: 1) Legend unit: mm.

REEL DIMENSIONS



ITEM	FOOTPRINT
Reel Diameter	13 inches
Reel Width(W1)	16.4mm

12.Version Description

REVISION	NOTES	DATE
Rev.0.0	Released datasheet	04-Jan-2023
Rev.0.1	Figures and description updated	28-Nov-2023
Rev.0.2	Safety-related certifications added	04-Jun-2024
Rev.0.3	Figures updated	09-Jul-2024
Rev.1.0	Power Ratings, Increased Safety-Limiting Values	31-Dec-2024
Rev.1.1	Increase Typical Characteristics、SOW-8 package information front view	09-Jun-2025

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest BASiC Semiconductor Office

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