2QP0225Txx

Description & Application Manual

RoHS
COMPLIANT

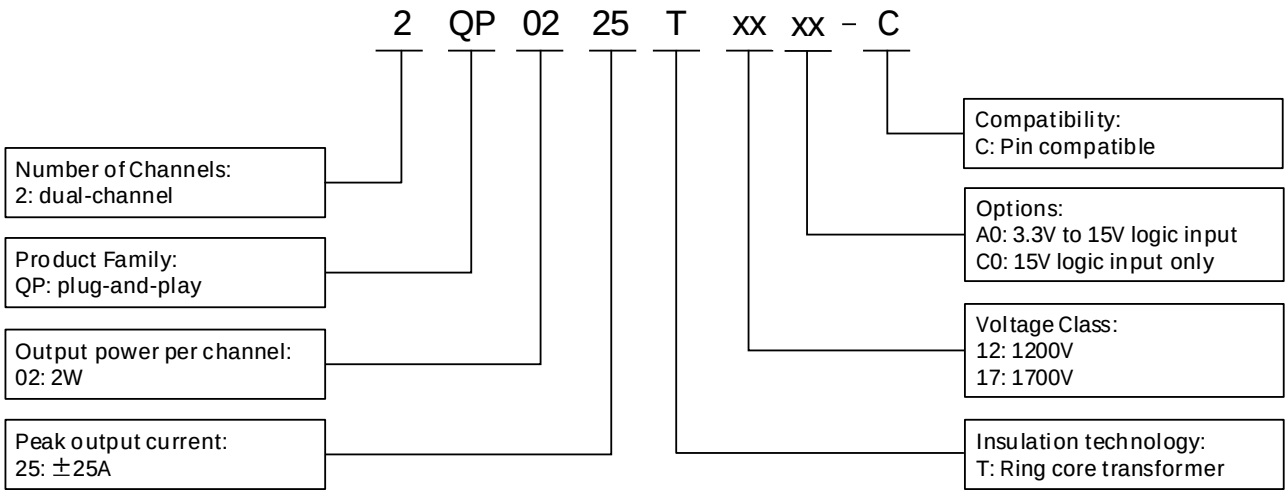
The photo is for reference only.

Description

2QP0225Txx is a dual-channel compact plug-and-play gate driver designed for high reliability applications based on the ASIC chipset developed by Bronze Technologies.
2QP0225Txx is suitable for 2-level topologies built with EconoDUAL™ package IGBT modules up to 1700V. The plug-and-play capability of the driver allows immediate operation without adaptions after assembly.

Contents

Nomenclature



Block Diagram Of Driver Board

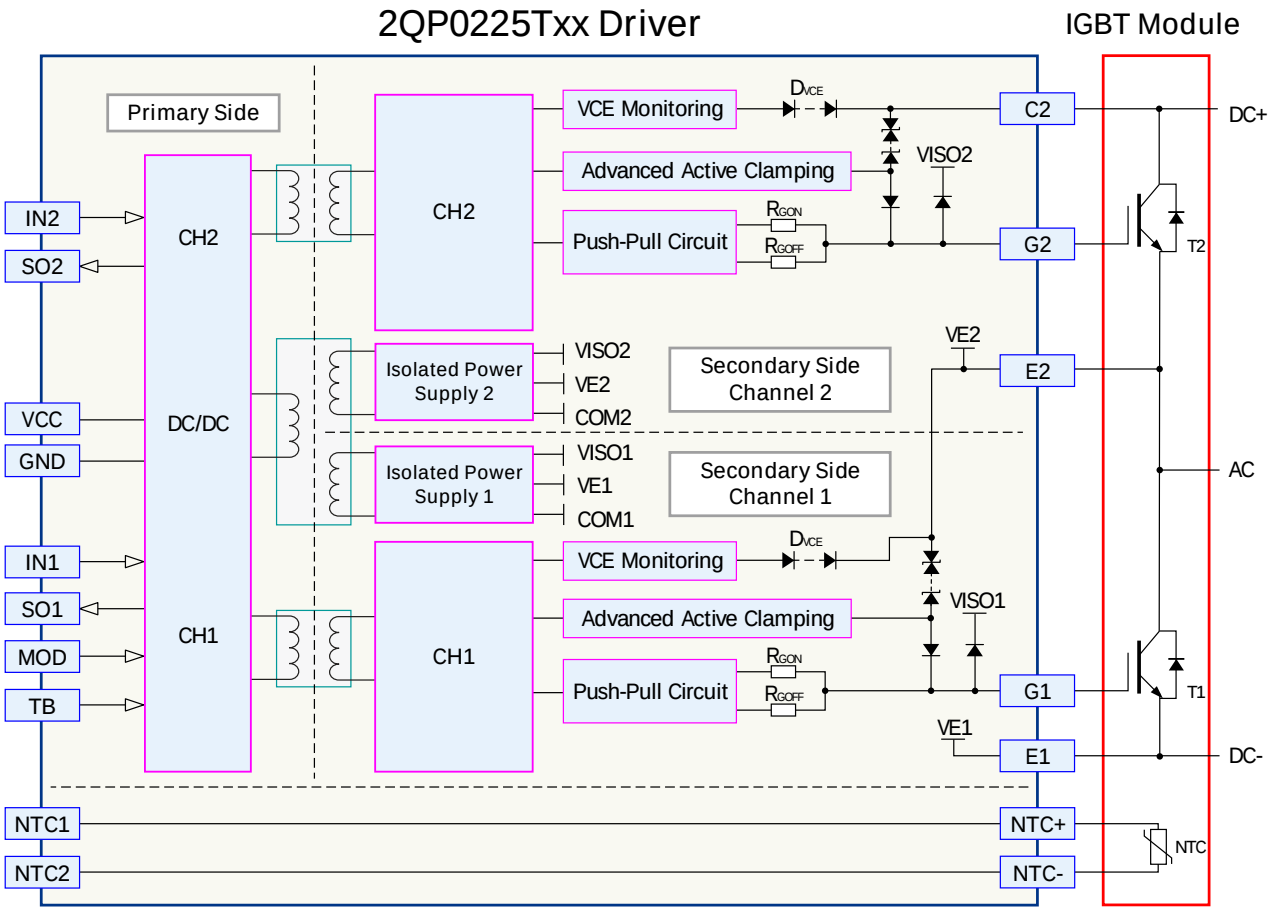


Figure 1. Block diagram of 2QP0225Txx

Recommended Interface Circuitry for Connector P1

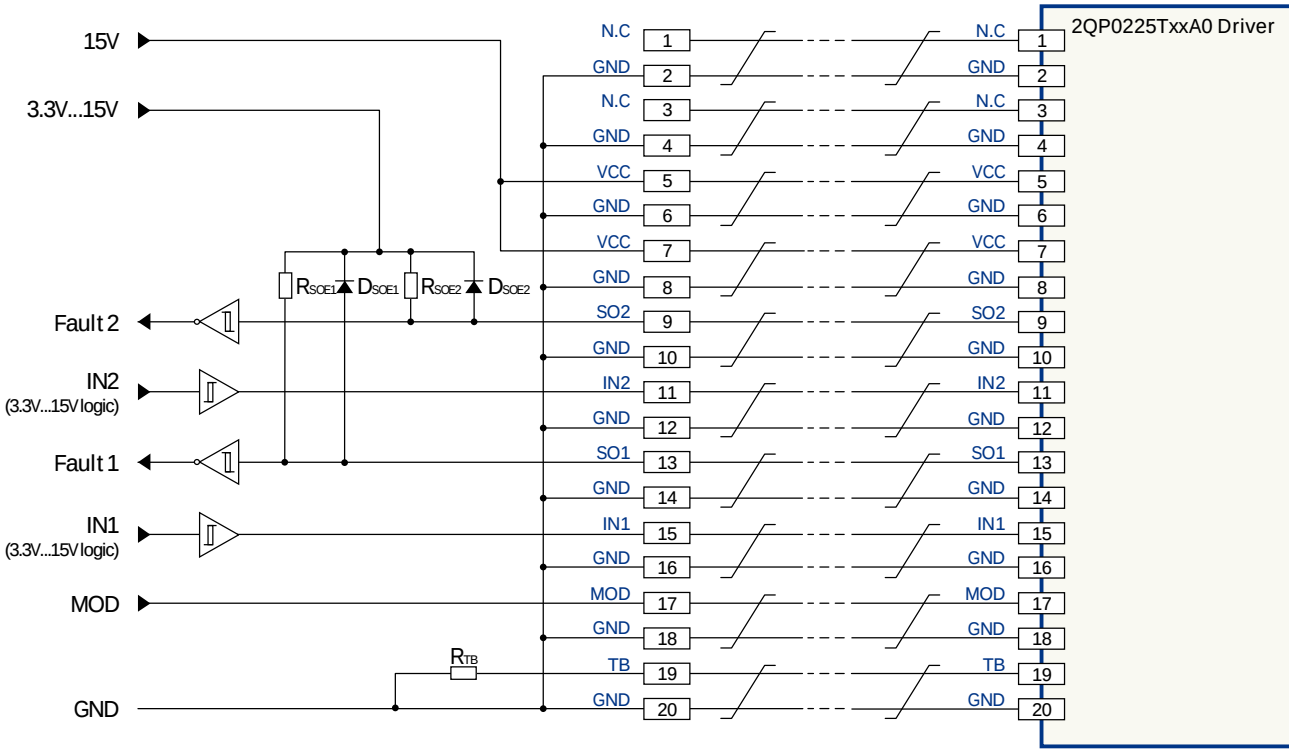


Figure 2. Recommended user interface of 2QP0225TxxA0

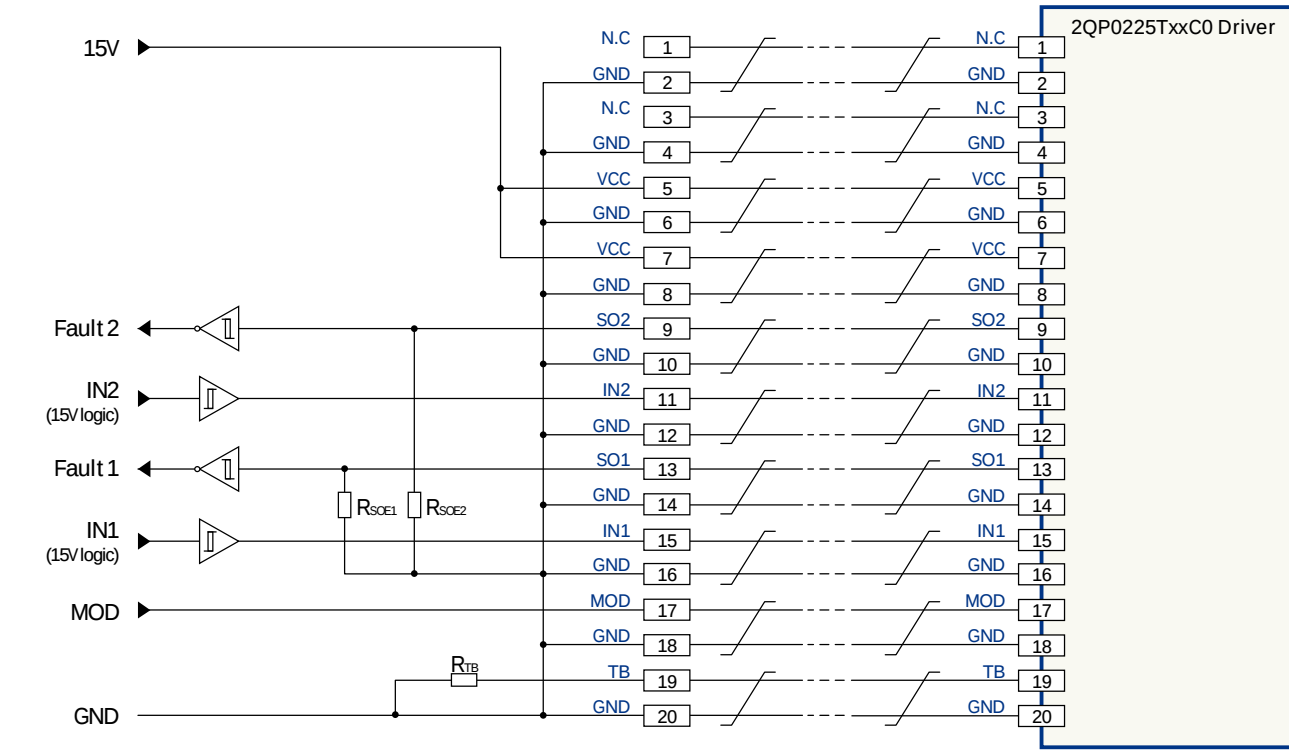


Figure 3. Recommended user interface of 2QP0225TxxC0

Direct Mode

MOD pin	IN		IGBT	
	IN1	IN2	Gate1	Gate2
Left open or connected to VCC	1	1	1	1
	0	1	0	1
	1	0	1	0
	0	0	0	0

Half-bridge Mode

MOD pin	IN		IGBT	
	IN1	IN2	Gate1	Gate2
Shorted to GND	1	1	1	0
	0	1	0	1
	1	0	0	0
	0	0	0	0

Block Diagram With Connection to IGBT Module

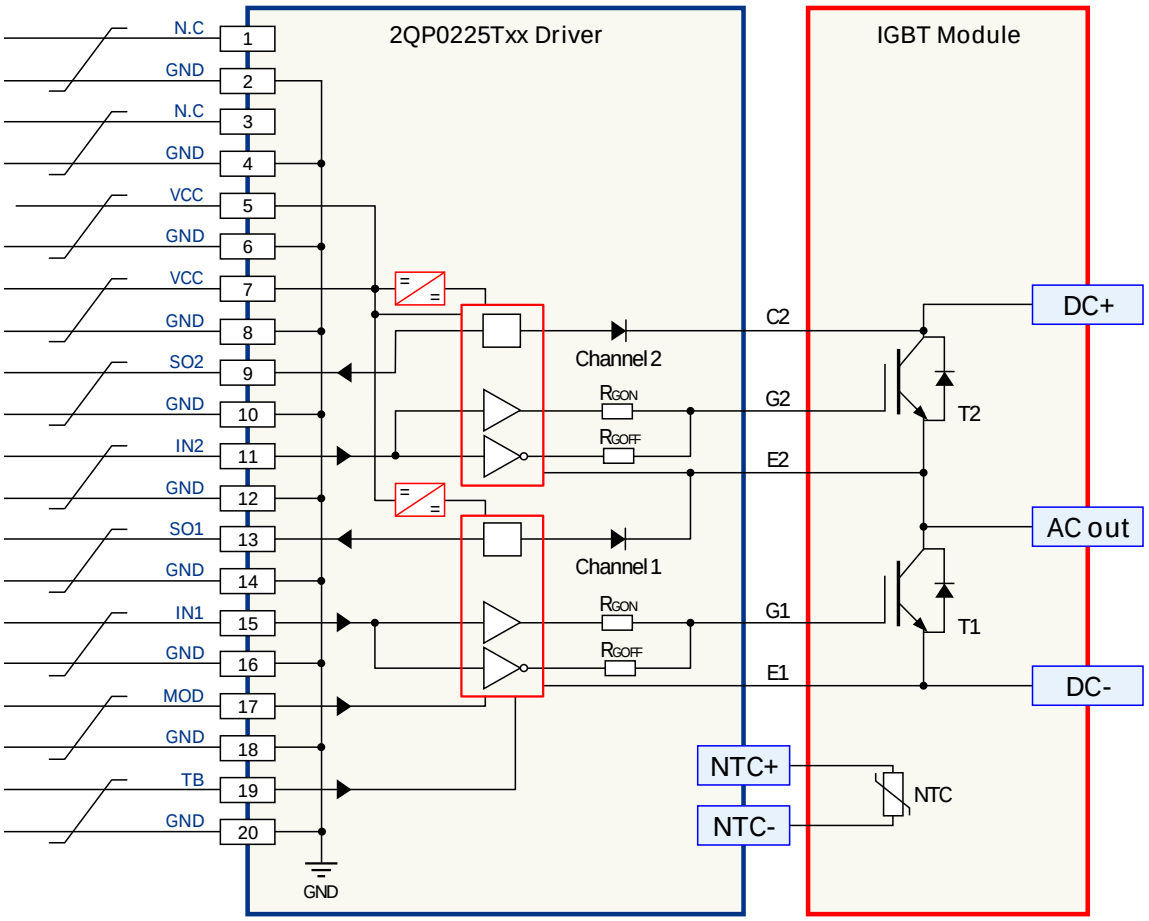


Figure 4. Block diagram covering driver 2QP0225Txx and IGBT module

Pin Designation

Connector P1[1)]

Pin	Symbol	Description	Pin	Symbol	Description
1	N.C	Not connected	2	GND	Ground
3	N.C	Not connected	4	GND	Ground
5	VCC	15V supply voltage	6	GND	Ground
7	VCC	15V supply voltage	8	GND	Ground
9	SO2	Status output channel 2	10	GND	Ground
11	IN2	Signal input channel 2	12	GND	Ground
13	SO1	Status output channel 1	14	GND	Ground
15	IN1	Signal input channel 1	16	GND	Ground
17	MOD	Mode selection (direct/half-bridge)	18	GND	Ground
19	TB	Set blocking time	20	GND	Ground

Note: 1) 20-pin shrouded socket with eject hooks is default configuration.
lt is recommended to use the flat cable connector 71600-020LF from FCL.

Connector P2

Pin	Symbol	Description
1	NTC1	Module NTC resistor terminal 1
2	NTC2	Module NTC resistor terminal 2

Note: 1) 2-pin shrounded connector with friction lock is default configuration.
It is recommended to use the connector 0022012027 from Molex.

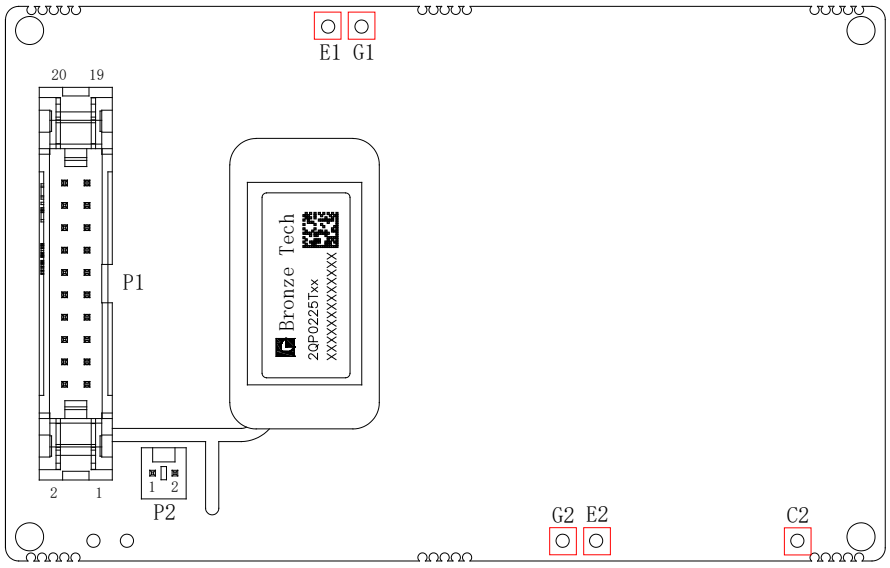


Figure 5. 2QP0225Txx Pin layout

Function Description

Power Supply and Monitoring

The DC/DC converter of the driver provides galvanic isolation between primary side power supply and secondary side gate driving circuitry.

Supply voltage monitoring is deployed for the primary-side and two secondary-sides of the DC/DC converter for undervoltage lockout (UVLO).

Note: A stable primary side supply voltage is required.

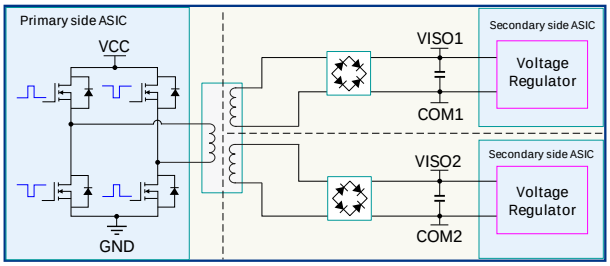


Figure 6. Power supply circuitry

Primary Side Supply Monitoring:

The supply voltage V_{CC} is monitored on the primary-side for undervoltage lockout. When V_{CC} drops to the UVLO set fault threshold V_{CCUV+}, UVLO is triggered, two secondary-side gate drive outputs are locked in off state and keep the IGBT off. Meanwhile, the fault signal SO1 and SO2 are pulled down.

When V_{CC} returns to the UVLO clear fault threshold V_{CCUVR+}, the driver continues to maintain the lockout state for a period t_B, then exits the lockout state and pulls up fault signals SOx.

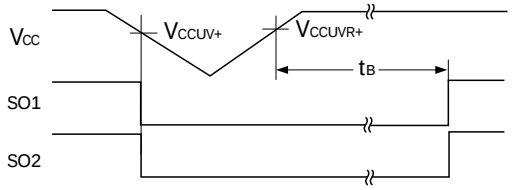


Figure 7. Primary-side UVLO logic

Secondary Side Supply Monitoring:

The secondary power supply voltage is also monitored to ensure a safe IGBT switching. To demonstrate the behavior of the secondary side UVLO, a scenario is considered in below where the primary side supply voltage V_{CC} decreases from the nominal value towards zero:

1) At first the positive voltage V+ (VISO to VE) is held constant on the nominal value, while the negative voltage V- (COM to VE) deviates from the nominal value towards zero along with the decreasing V_{CC}.

2) As soon as V- reaches -5V, V- is held constant and V+ starts to fall towards zero if V_{CC} further collapses.

3) When V+ reaches the set fault threshold V_{UV+}, UVLO protection is initiated. The IGBT is turned off and held in off state, meanwhile a set fault signal is transmitted to the primary side and asserts SOx pin immediately.

4) The counting of t_B starts when a UV fault is detected. This is different from the primary side supply voltage monitoring, where the counting of t_B starts after UV fault is cleared. If a new fault is detected before t_B of the previous fault elapses, t_B is recounted from the new fault.

5) When Vcc rises again, the driver firstly restores V+.

6) If V+ further increases and reaches its nominal value, V+ is held constant and V- starts to recover towards its nominal value.

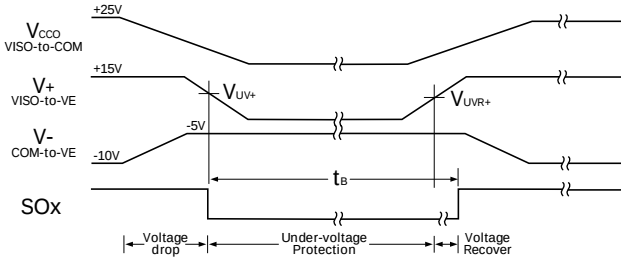


Figure 8. Secondary-side UVLO logic

Input Signal

The triggering signal is input from INx port. The turn-on threshold V_{INH} and turn-off threshold V_{INL} are defined by different resistor configurations on the driver board.

Part Number	R_{INx1}	R_{INx2}	R_{INx3}
2QP0225TxxA0-xx	4.7kΩ	Unassembled	1kΩ
2QP0225TxxC0-xx	Unassembled	1.2kΩ	3.3kΩ

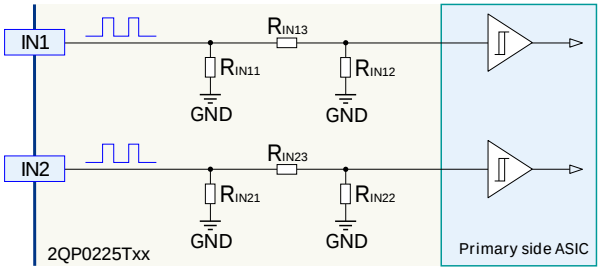


Figure 9. INx input circuitry

Transmission Logic and Mode Selection

The driver can be configured as direct or half-bridge mode. Operating mode of the driver can be configured by the MOD pin connection.

Direct Mode:

If the MOD pin is left open or connected to VCC, direct mode is selected and the two channels are independent. Input IN1 corresponds to Channel 1, while input IN2 corresponds to Channel 2. A logic high turns on the corresponding IGBT, while a logic low turns it off.

Note: In direct mode, make sure to add a proper dead time in the input signals to avoid shoot-through of the two switches in a bridge.

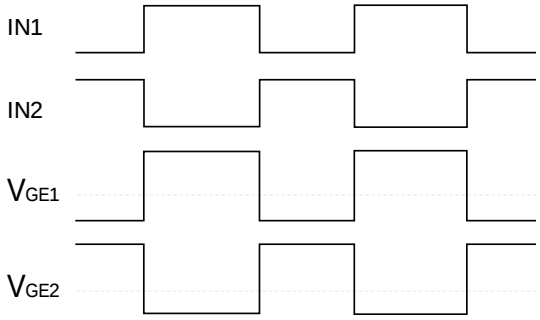


Figure 10. Transmission logic in direct mode

Half-Bridge Mode:

If the MOD pin is shorted to ground, the driver operates in half-bridge mode. In this mode, IN1 serves as PWM signal and IN2 as enabling signal.

When IN2 is low, both channels are locked in off state. If IN2 is high, both channels are enabled. The gate output signals of both channels are determined by IN1. At the transition of IN1 from low to high, the gate output of Channel 2 is turned off immediately. After a dead time DT elapses, the gate output of Channel 1 is turned on. At the transition of IN1 from high to low, the gate output of Channel 1 is turned off immediately. After the dead time DT elapses, the gate output of Channel 2 is turned on.

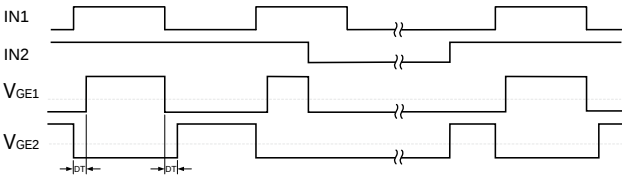


Figure 11. Transmission logic in Half-bridge mode

Status Output Signal

The output SOx has open-drain transistor on the driver board.

Part Number	RSOx1	RSOx2
2QP0225TxxA0-xx	33Ω	Unassembled
2QP0225TxxC0-xx	33Ω	10kΩ

2QP0225TxxA0-xx:

When no fault is detected, Q_{SOx} keeps off, the outputs SOx have high impedance. When a fault is detected, the corresponding SOx is pulled down to ground.

It is recommended to mount external pull-up resistors as demonstrated in the diagram of recommended user interface of 2QP0225TxxA0-xx. The diodes D_{SOEx} are only required when using 3.3V input logic level. For 5V…15V logic, they can be omitted.

In a fault condition, the maximum SOx current must not exceed 20mA.

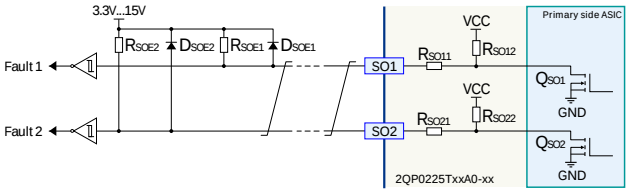


Figure 12. SOx user interface of 2QP0225TxxA0-xx

2QP0225TxxC0-xx:

When there is no fault, Q_{SOx} keeps off, and each of the SOx is pulled up to VCC via a resistor on the driver board. When a fault is detected, the corresponding SOx is pulled down to ground. It is recommended to assemble external pull down resistors R_{SOEx} to ground as demonstrated in the diagram of recommended user interface of 2QP0225TxxC0-xx, which allows a missing SOx connection to be detected (safe logic in the event of a defective cable). Note that R_{SOEx} (pull down resistor on the user's board) must have sufficiently high resistance (e.g. 150 kΩ), as they form a voltage divider together with the internal pull-up resistor (typically 10kΩ) on the driver board.

SO1 and SO2 can be connected together to provide fault information of the entire driver. However, for fast and precise fault diagnosis, it is recommended to detect the information independently.

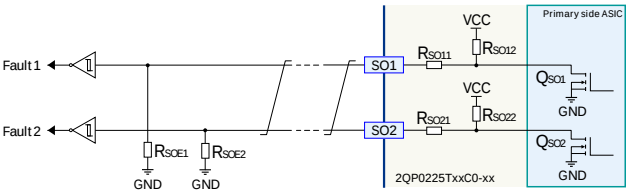


Figure 13. SOx user interface of 2QP0225TxxC0-xx

Blocking Time Setting

The blocking time t_B can be configured by an external resistor R_{TB} between TB pin and GND.

The following formula describes the relationship between t_B and R_{TB} (at typical values).

$$R_{TB}[ms] = \frac{8250+150 \cdot t_B[ms]}{95-t_B[ms]}$$

($R_{TB} \geqslant 150k\Omega$, $20ms \leqslant t_B \leqslant 95ms$)

When R_{TB} is 150kΩ , the blocking time t_B is 20ms. When TB is left open, the blocking time is 95ms.

Note: R_{TB} should not be smaller than 150kΩ, which means the blocking time t_B cannot be shorter than 20ms, otherwise the blocking time t_B will be inaccurate and unstable. If TB pin is shorted to ground, t_B is fixed to 10us.

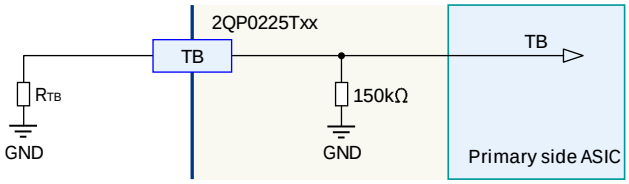


Figure 14. Blocking time setting

IGBT Turn-on and Turn-off

To turn on the IGBT, Q_{ON} is turned on, Q_{OFF} is turned off, and then the gate resistor R_{GON} is pulled up to charge the IGBT gate. Thus to turn on the IGBT.

To turn off the IGBT, Q_{OFF} inside the ASIC of the driver is turned on, and Q_{ON} is turned off, the gate resistor Q_{OFF} is pulled down to discharge the IGBT gate. Thus to turn off the IGBT.

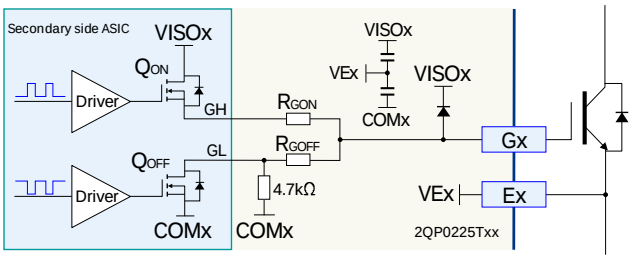


Figure 15. Gate drive output circuitry

Active Clamping

Fast IGBT turn-off may lead to voltage spikes, which is critical when DC-link voltage and load current are high. Voltage spikes can cause damage to the IGBT. The turn-off voltage spike is mainly correlated to the stray inductance L_S and the slew rate of the IGBT turn-off current di/dt. By adjusting the turn-off gate resistor R_{GOFF}, di/dt can be reduced and the voltage overshoot is reduced. However, the impact of L_S is inevitable. It can be more pronounced under high current in short circuit or overload. The driver is equipped with active clamping function to effectively prevent the overvoltage damage on IGBT.

A feedback path from the IGBT collector to the gate is established using transient voltage suppressor devices (TVS).When the V_{CE} peak voltage exceeds the breakdown threshold, the TVS chain will break through and the current through it will charge the IGBT gate, which turns on the IGBT partially and suppresses the excessive V_{CE} of the IGBT.

Part Number	IGBT Voltage	TVS Chain Breakdown Threshold @ 25°C
2QP0225T12xx	1200V	912V
2QP0225T17xx	1700V	1320V

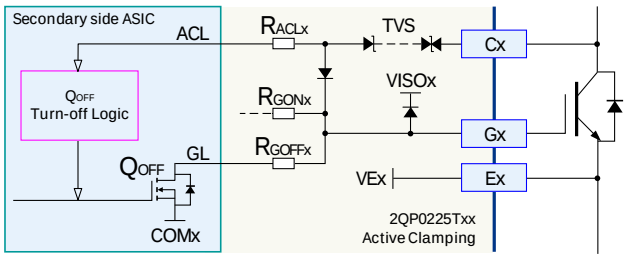


Figure 16. Active clamping circuitry

IGBT Short-Circuit Protection

The V_{CE} detection circuitry is used for IGBT short-circuit protection. The detection of two channels are independent from each other. The short-circuit detection is only valid when the IGBT is turned on. When the IGBT is in off state, the input signal turns on Q_{CEx} and clamps V_{CEDTx} to COMx. In this case, the comparator outputs logic low.

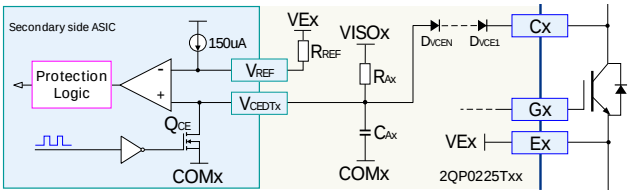


Figure 17. Short-circuit protection circuitry

Normal Turn-On:

When the logic input will turn on the IGBT, Q_{CE} is firstly turned off and releases the clamping of V_{CEDTx}. At this moment, IGBT is still in off state and V_{CE} is high. C_{Ax} capacitor is charged through the resistor R_{Ax}, V_{CEDTx} rises. Then the IGBT is turned on, V_{CE} quickly drops to saturation voltage V_{CE-SAT} and V_{CEDTx} reaches V_{CE-SAT}.

As V_{CE-SAT} is significantly lower than the protection threshold V_{REF}, the comparator does not flip over and the protection is not initiated.

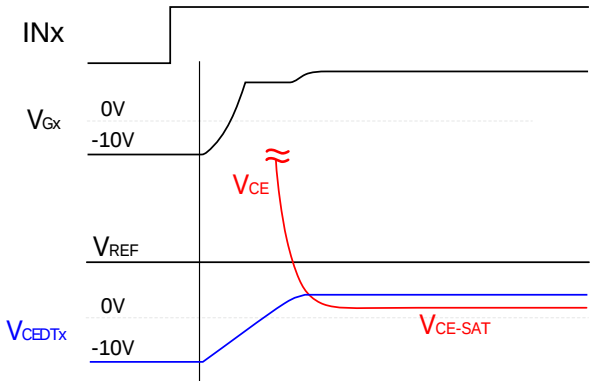


Figure 18. Signal waveform at normal turn-on

Class I Short-Circuit Protection:

When Class I short circuit (bridge shoot-through) occurs, due to the rapid increase of the short cirucit current, the IGBT desaturates and result in rapidly increased V_{CE}. C_{Ax} is charged and V_{CEDTx} rises until it is clamped at VISOx. During this process, V_{CEDTx} exceeds V_{REF} and the comparator's output flips, which consequently triggers the short-circuit protection.

The short-circuit protection logic turns off the IGBT immediately to ensure its safety. At the same time, set fault signal is sent to the primary side to pull down the SOx pin, so as to alert a fault state. The channel is locked in fault state for a period t_B before recovering to the normal state.

The protection circuits of the two channels are independent from each other. Therefore, when short-circuit protection is initiated on one channel, the other channel remains operating normally. It is recommended to check the SOx signal timely and activate system lockout when necessary.

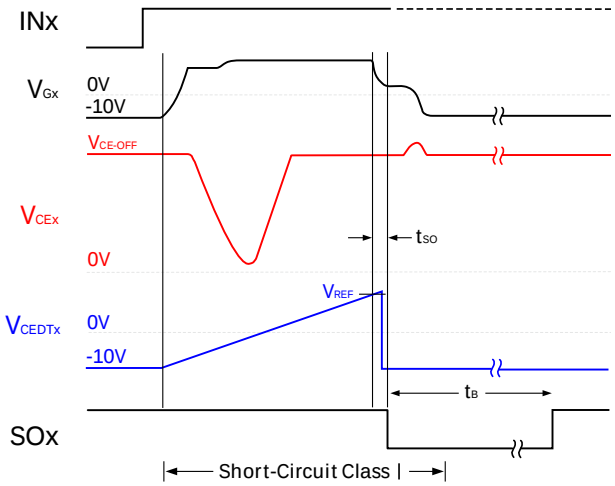


Figure 19. Class I short-circuit protection

Class II Short-Circuit Protection:

When a Class II short circuit (e.g. phase to phase short circuit) occurs, the current ramps up slowly as the short circuit impedance is relatively high. The IGBT still enters saturation state normally. As the short-circuit current increases, V_{CE} increases gradually until it exceeds the protection threshold, then the driver initiate short-circuit protection. The response time in Class II short-circuit protection is longer than that of Class I.

In another case, if bridge shoot-through occurs under low DC-link voltage, the short circuit current is low and also resulting in increased protection response time.

Note: When a Class II short circuit occurs, the short circuit impedance varies greatly, which leads to uncertain timing of IGBT desaturation. Therefore, before the protection is initiated, the IGBT may have been already damaged by a considerable sum of heat accumulated. In this case, the driver's short-circuit protection cannot guarantee the intactness of the IGBT. Extra overcurrent protection measures have to be introduced.

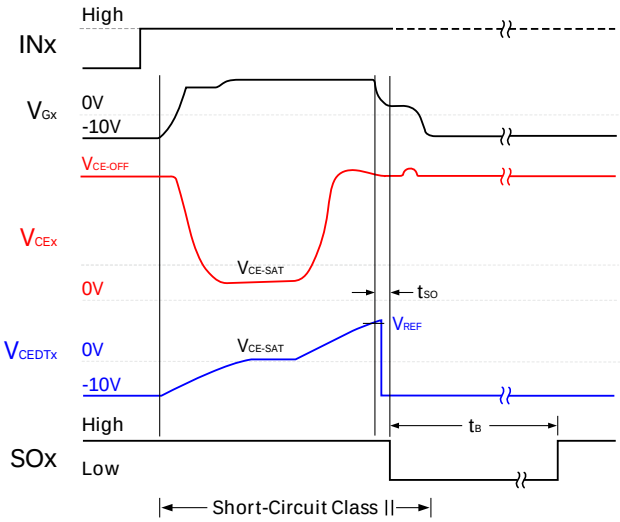


Figure 20. Class II short-circuit protection

Soft Shut Down

Due to the stray inductance, excessive voltage spikes are generated when the short-circuit of IGBT is turned off. In order to suppress voltage spikes without affecting the speed of turn-off during normal operation, it is necessary to deploy soft shut down function.

The secondary-side ASIC of the driver has an embedded soft shut down function. When fault condition is detected, soft shut down function is activate to protect the IGBT.

The mechanism is described below:

1) When fault is detected (short circuit or undervoltage), the Q_{ON} is turned off immediately by the protection function, while Q_{OFF} remains off, thus the gate voltage of the IGBT is unchanged.

2) An internally generated voltage reference V_{REF_SSD} drops with a pre-defined slope. As the gate votlage is unchanged, there is a difference between V_{GH} and V_{REF_SSD}, thus the hysteresis comparator generates a positive output.

3) The Q_{OFF} is turned on by the comparator output, the gate voltage and V_{GH} gradually drop. When V_{GH} drops too fast, so that V_{GH} becomes lower than V_{REF_SSD}, Q_{OFF} is turned off untill V_{REF_SSD} falls below V_{GH}. The aforementioned process is repeated.

4) In this way, the gate voltage drops with the same trend as V_{REF_SSD} to ensure soft shut down.

The soft shut down period is fixed at 2.0 us. When gate voltage drops to 0V, Q_{OFF} is kept on to pull V_{GL} directly to COMx.

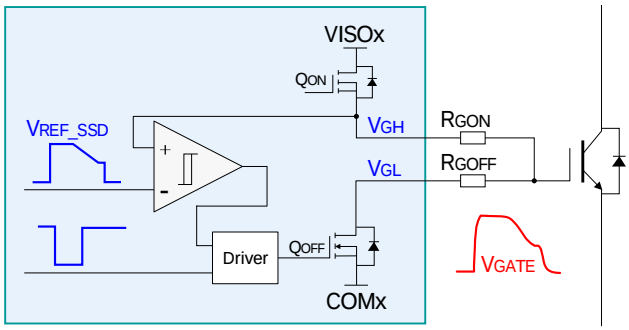


Figure 21. Soft Shut Down

Mechanical Dimensions

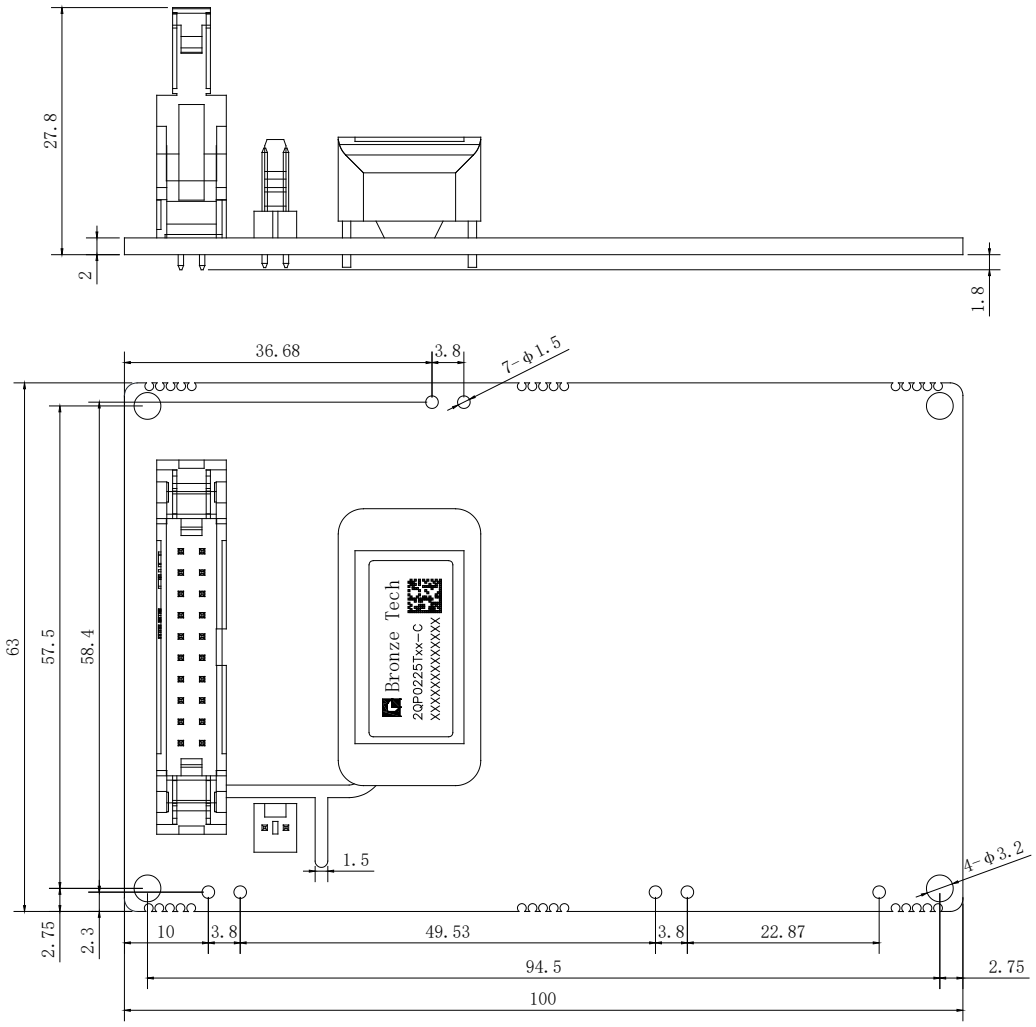


Figure 22. Mechanical drawing of 2QP0225Txx

Note: 1)Legend unit: mm.
2)The margin tolerance conforms with the ISO 2768-1.

Revision History

REVISION	NOTES	DATE
V1. 0	Intial release	10-Oct-2023

Precautions

- All operations on the IGBT module and driver shall conform with the electrostatic-sensitive device (ESD) protection requirements stipulated in IEC 60747-1/IX or EN100015.
- To protect ESDs, IGBT module and driver operation, including the operation sites and tools, must conform with these standards.

The IGBT and driver may be damaged due to negligence in ESD protection.

- Before powering on the driver, make sure that the driver and control board are connected correctly, without empty connection, false connection, or false soldering.
- After the driver is installed, its surface voltage to the ground may exceed the safety voltage. Therefore, do not touch it with bare hands.

Operations may involve life hazards. Be sure to follow the corresponding safety protocols !

DISCLAIMER

The technologies and reliability data (including datasheets), design resources (including 3D models, structure diagrams, and AD models), application notes, application programs, and other design recommendations, tools, safety information and resources provided by Bronze Technologies do not constitute any guarantees, implicit or explicit, on the delivery, function, specific usage, applicability, or no infringement on a third party's intellectual property rights.

These resources are intended for engineers specialized in product development upon Bronze Technologies products, who are fully responsible for:

1)Choosing appropriate Bronze Technologies products for your products;

2)Design, verification, and testing of your products;

3)Ensuring that your products meet applicable requirements.

The data, documents, and resources are subject to regular updates without notification. Please visit BronzeTechnologies'website www.qtjtec.com or WeChat official account for the latest resources.

You are authorized to use the resources only when you use the corresponding Bronze Technologies products, and however are prohibited from replicating or demonstrating these resources in other means. These resources do not constitute authorization of intellectual property rights of Bronze Technologies or a third party to any party. Bronze Technologies assumes no liability in any claims, damages, losses, or costs incurred during your use of these resources and is entitled to recovery of losses caused by infringement of intellectual property rights.

Bronze Tech Group | Shenzhen Bronze Technologies Ltd.

Website: www.qtjtec.com
Technical Support Tel.: +86 0755 33379866
Technical Support Email: support@qtjtec.com

Scan QR code to enter Bronze website.